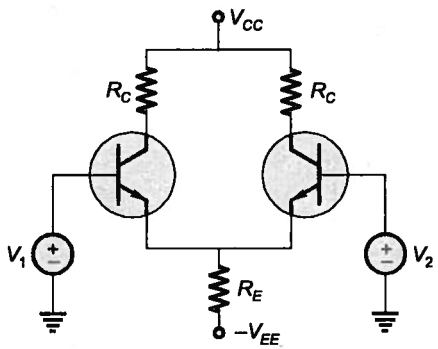
9 Op-Amps and 555 Timer

Multiple Choice Questions

Q.1 In an ideal differential amplifier shown in figure, a large value of R_E



(a) increases both differential and common mode pairs
(b) increases the common mode gain only
(c) decreases the differential mode gain only
(d) decrease the common mode gain only

Q.2 A change in the value of emitter resistance R_e in a difference amplifier
(a) affects A_d
(b) affects A_c
(c) affects both A_d and A_c
(d) does not affect either A_d or A_c

Q.3 In a differential amplifier, CMRR can be improved by using an increased
(a) emitter resistance
(b) collector resistance
(c) power supply voltage
(d) source resistance

Q.4 A differential amplifier has inputs $V_1 = 1050\ \mu V$ and $V_2 = 950\ \mu V$ with CMRR = 1000, what is the error in differential output?
(a) 10% (b) 1%
(c) 0.1% (d) 0.01%

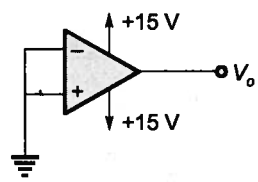
Q.5 The differential gain of op-amp is 4000 and value of CMRR is 150. Its output voltage, when the two input voltages are 200 μV and 160 μV respectively, will be
(a) 16 V (b) 164.8 mV
(c) 64 mV (d) 76 mV

[ESE-2014]

Q.6 Consider the following statements:
1. A differential amplifier is used at the input stage of an operational amplifier.
2. Differential amplifiers have very high CMRR.
Which of these statements are correct?
(a) Both 1 and 2 (b) Neither 1 nor 2
(c) 1 only (d) 2 only

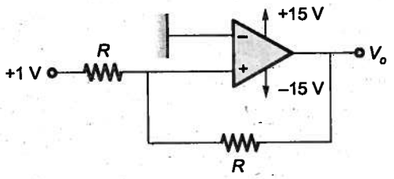
[ESE-2013]

Q.7 The op-amp in the figure has an input offset voltage of 5 mV and an open loop voltage gain of 10000, then V_o will be



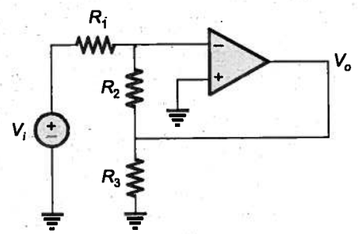
(a) 0 (b) 5 mV
(c) +15 V or –15 V (d) +50 V or – 50 V

Q.8 In the circuit of figure, V_o is



(a) –1 V (b) 2 V
(c) +1 V (d) +15 V

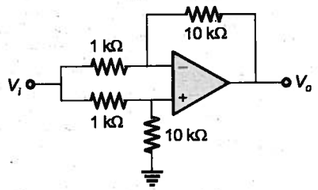
Q.9 Assuming the op-amp to be ideal. The voltage gain of the amplifier shown below is



(a) $-\frac{R_2}{R_1}$ (b) $-\frac{R_3}{R_1}$

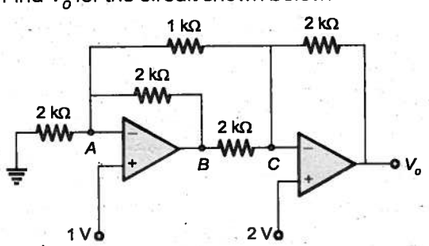
(c) $-\left(\frac{R_2 \| R_3}{R_1}\right)$ (d) $-\left(\frac{R_2 + R_3}{R_1}\right)$

Q.10 The V_o of the op-amp circuit shown is



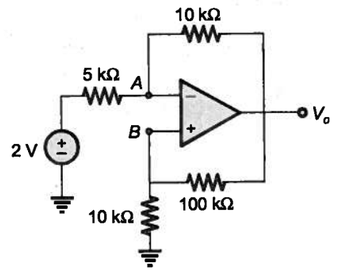
(a) 11 V_i (b) 10 V_i
(c) V_i (d) zero

Q.11 Find V_o for the circuit shown below:



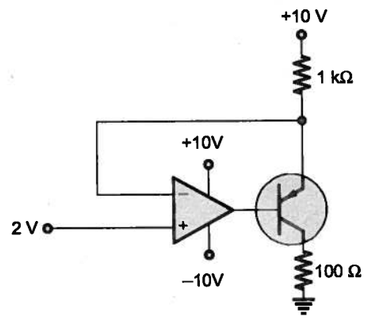
(a) 6 V (b) 15 V
(c) 10 V (d) 18 V

Q.12 The output voltage V_o of the circuit is



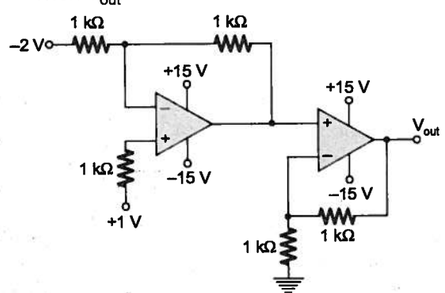
(a) –4 V (b) 6 V
(c) 5 V (d) –5.5 V

Q.13 In the circuit shown in the figure the current flowing through resistance of 100 Ω would be



(a) 8 mA (b) 10 mA
(c) 20 mA (d) 100 mA

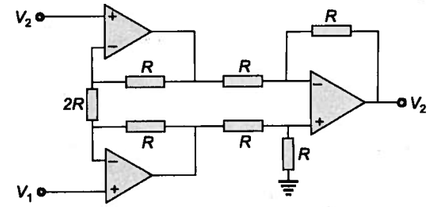
Q.14 In the circuit shown below the op-amps are ideal. Then V_{out} in Volts is



(a) 4 (b) 6
(c) 8 (d) 10

[GATE-2013]

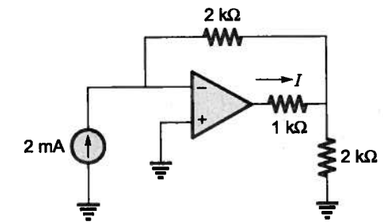
Q.15 Given that the op-amps in the figure are ideal, the output voltage V_0 is



(a) $(V_1 - V_2)$ (b) $2(V_1 - V_2)$
(c) $\frac{(V_1 - V_2)}{2}$ (d) $(V_1 + V_2)$

[GATE-2014]

Q.16 Assume the op-amp to be ideal. The current I through 1 kΩ resistor is

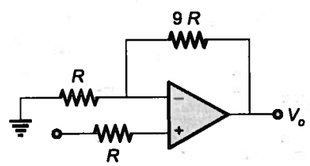


(a) –2 mA (b) –4 mA
(c) –6 mA (d) –8 mA

Q.17 The data sheet of an op-amp gives a mid band voltage gain of 200000 with a cut-off frequency of 10 Hz. What is the voltage gain at 1 MHz?

(a) 2 (b) 3.2
(c) 1 (d) 0

Q.18 The bandwidth of an amplifier circuit given below is. It is given that 0 dB product of the op-amp is 1 MHz.



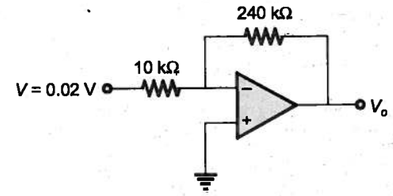
(a) 10^5 Hz (b) 10^7 Hz
(c) 10^4 Hz (d) none

Q.19 An amplifier using an opamp with a slew-rate SR = 1 V/μsec has a gain of 40 dB. If this amplifier has to faithfully amplify sinusoidal signals from dc to 20 kHz without introducing any slew-rate induced distortion, then the input signal level must not exceed.

(a) 795 mV (b) 395 mV
(c) 79.5 mV (d) 39.5 mV

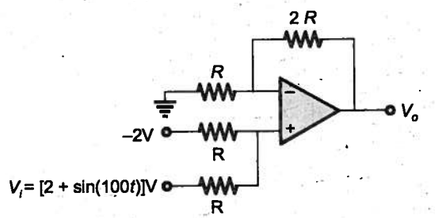
[GATE-2002]

Q.20 For the op-amp circuit given below determine the maximum input signal frequency in rad/sec. that can be used to get an distortionless output by taking SR 0.5 V/μsec.



(a) 1.04×10^6 rad/sec
(b) 2.04×10^6 radsec
(c) 1.32×10^4 rad/sec
(d) 0.26×10^5 rad/sec

Q.21 A non-inverting op-amp is shown below (assume ideal op-amp)

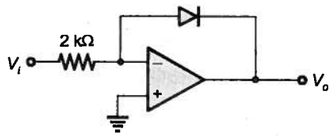


The output voltage V_o for an input
$V_i = [2 + \sin(100t)]$ V

(a) 3/2 sin (100 t) (b) 3 sin (100 t)
(c) 2 sin (100 t) (d) 3 sin (100 t) +1/2

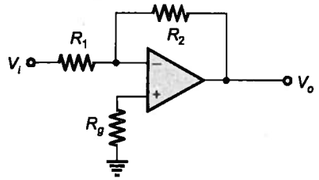
[ESE-2002]

Q.22 In the Op-Amp circuit shown, assume that the diode current follows the equation $I = I_s \exp(V/V_T)$. For $V_i = 2$ V, $V_o = V_{01}$, and for $V_i = 4$ V, $V_o = V_{02}$. The relationship between V_{01} and V_{02} is



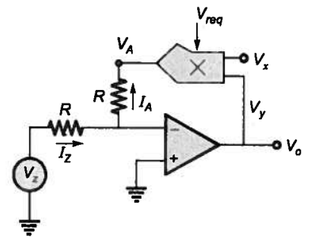
(a) $V_{02} = \sqrt{2}\, V_{01}$
(b) $V_{02} = e^2\, V_{01}$
(c) $V_{02} = V_{01}\, In\, 2$
(d) $V_{01} - V_{02} = V_T\, In\, 2$ **[GATE-2007]**

Q.23 In the inverting op-amp circuit shown below, the resistance R_g is chosen as $R_1 \parallel R_2$ in order to



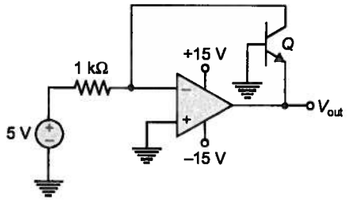
(a) increase gain
(b) reduce offset voltage
(c) reduce offset current
(d) increase CMRR **[ESE-2002(EE)]**

Q.24 Find V_0 for the circuit shown below:



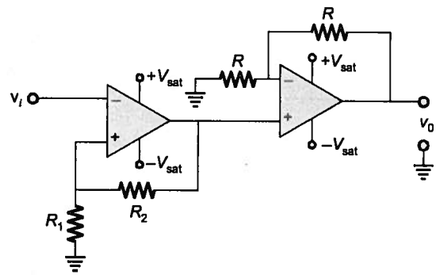
(a) $-V_{req}\dfrac{V_z}{V_x}$ (b) $-V_{req}\dfrac{V_x}{V_z}$
(c) $-V_{req}\, V_z$ (d) $-V_{req}\, V_x$

Q.25 In the circuit shown below what is the output voltage (V_{out}) if a silicon transistor Q and an ideal op-amp are used?



(a) −15 V (b) −0.7 V
(c) +0.7 V (d) +15 V **[GATE-2013]**

Q.26 An operational amplifier circuits is shown in the figure.



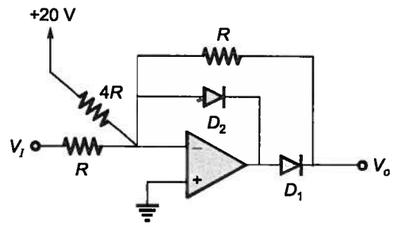
The output of the circuit for a given input v_i is

(a) $-\left(\dfrac{R_2}{R_1}\right)v_i$ (b) $-\left(1+\dfrac{R_2}{R_1}\right)v_i$

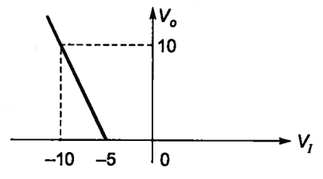
(c) $\left(1+\dfrac{R_2}{R_1}\right)v_i$ (d) $+V_{sat}$ or $-V_{sat}$

[GATE-2014]

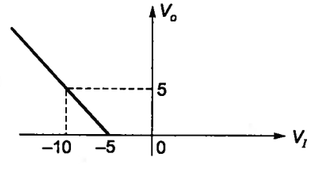
Q.27 The transfer characteristic for the precision rectifier circuit shown below is (assume ideal OP-AMP and practical diodes)



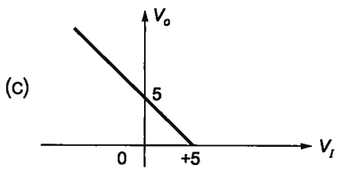
(a)



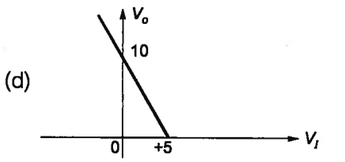
(b)



(c)

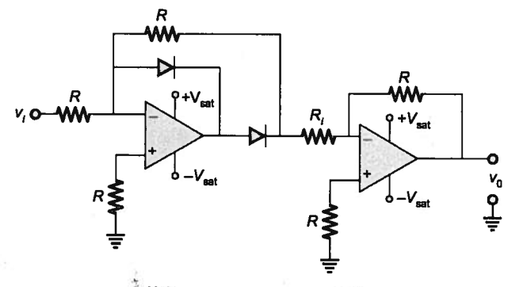


(d)

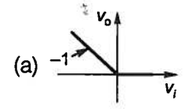


[GATE-2010]

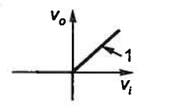
Q.28 The transfer characteristic of the op-amp circuit shown in figure is



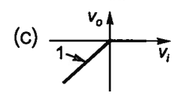
(a)



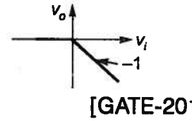
(b)



(c)

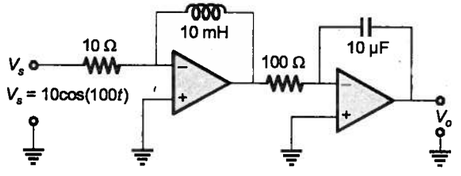


(d)



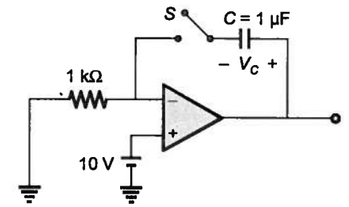
[GATE-2014]

Q.29 In the figure assume the OP-AMPs to be ideal. The output v_0 of the circuit is



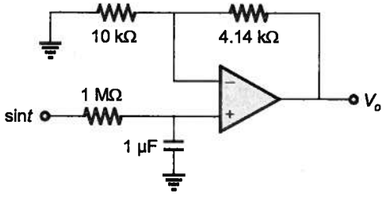
(a) $10\cos(100t)$
(b) $10\int_0^t \cos(100\tau)\, d\tau$
(c) $10^{-4}\int_0^t \cos(100\tau)d\tau$
(d) $10^{-4}\dfrac{d}{dt}\cos(100t)$ **[GATE-2001]**

Q.30 For the circuit shown in the following figure, the capacitor C is initially uncharged. At $t = 0$, the switch S is closed. The voltage V_C across the capacitor at $t = 1$ millisecond is (The Op-Amp is supplied with ±15 V.)



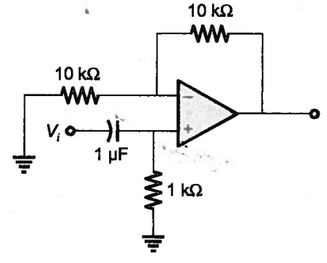
(a) 0 Volt (b) 6.3 Volts
(c) 9.45 Volts (d) 10 Volts **[GATE-2006]**

Q.31 In the circuit shown in the given figure, V_o is given by



(a) $\sin(t-\pi/4)$ (b) $\sin(t+\pi/4)$
(c) $\sin t$ (d) $\cos t$ **[ESE-2001]**

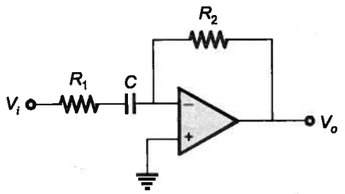
Q.32 The Op-amp circuit shown in the figure is a filter. The type of filter and its cut-off frequency are respectively



(a) high pass, 1000 rad/sec.
(b) low pass, 1000 rad/sec.
(c) high pass, 10000 rad/sec.
(d) low pass, 10000 rad/sec.

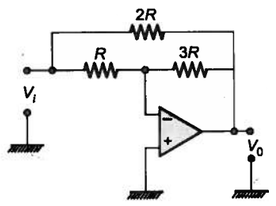
[GATE-2005]

Q.33 For the circuit shown in figure, the type of filter is



(a) Low pass (b) Band pass
(c) Band reject (d) High pass

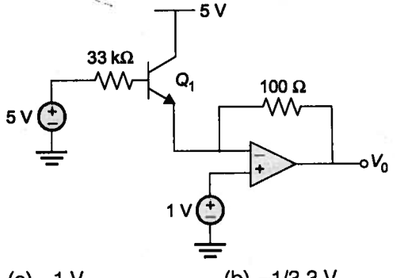
Q.34 The input resistance of the circuit shown in the figure, assuming an ideal op-amp is



(a) $\frac{R}{3}$ (b) $\frac{2R}{3}$
(c) R (d) $\frac{4R}{3}$

[GATE-2009]

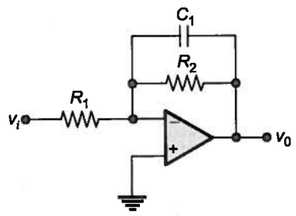
Q.35 Assuming base-emitter voltage of 0.7 V and $\beta = 99$ of transistor Q_1, the output voltage V_0 in the ideal opamp circuit shown below is



(a) –1 V (b) –1/3.3 V
(c) 0 V (d) 2 V

[GATE-2011]

Q.36 An active filter is shown in the adjoining figure. The dc gain and the 3 dB cut-off frequency of the filter respectively, are nearly

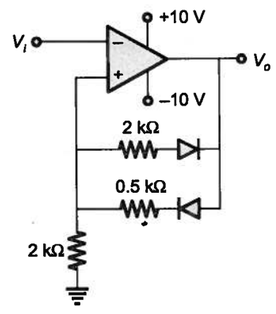


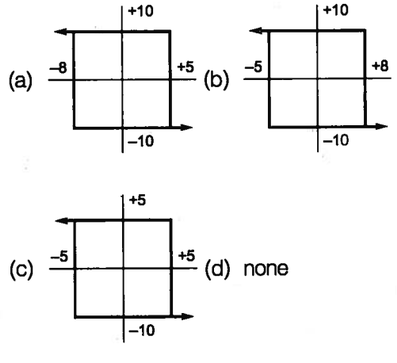
$R_1 = 15.9\ k\Omega$, $R_2 = 159\ k\Omega$,
$C_1 = 1.0\ nF$

(a) 40 dB, 3.14 kHz (b) 40 dB, 1.00 kHz
(c) 20 dB, 6.28 kHz (d) 20 dB, 1.00 kHz

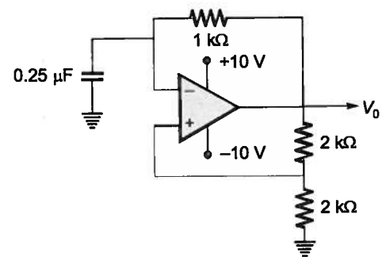
[GATE-2010]

Q.37 Given the ideal op-amp shown in figure indicate correct transfer characteristics assuming ideal diode with zero cut-in voltage





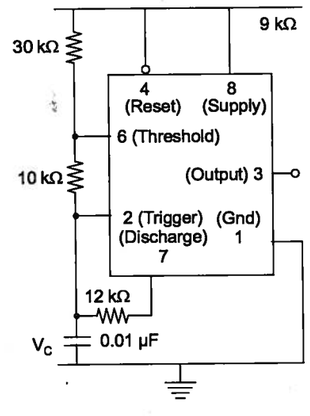
Q.38 The saturation voltage of the ideal op-amp shown below is ±10 V. The output voltage n_0 of the following circuit in the steady-state is



(a) square wave of period 0.55 ms
(b) triangular wave of period 0.55 ms
(c) square wave of period 0.25 ms
(d) triangular wave of period 0.25 ms

[GATE-2015]

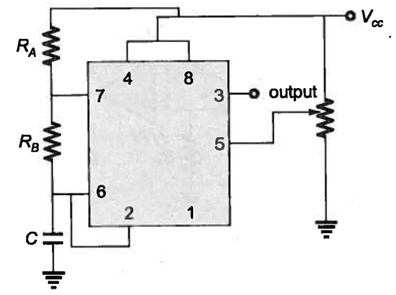
Q.39 An astable multi-vibrator circuit using IC 555 timer is shown below. Assume that the circuit is oscillating steadily.



The voltage V_C across the capacitor varies between
(a) 3 V to 5 V (b) 3 V to 6 V
(c) 3.6 V to 6 V (d) 3.6 V to 5 V

[GATE-2008]

Q.40 Circuit shown in the figure represents

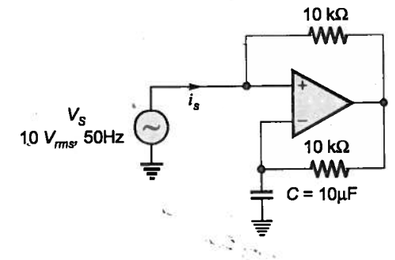


(a) astable multivibrator
(b) a mono stable multi vibrator
(c) voltage controlled oscillator
(d) ramp generator

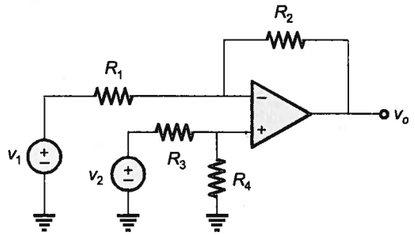
Numerical Data Type Questions

Q.41 Consider an inverting amplifier circuit having gain of –100 is designed using an op-amp and two resistors $R_1 = 10\ k\Omega$ and $R_2 = 1\ M\Omega$. If the op-amp is specified to have input bias current of 100 nA and input offset current of 10 nA then the output dc offset voltage will be = _____ V. Assume bias current at inverting terminal is greater than bias current at non-inverting terminal.

Q.42 The following circuit has $R = 10\ k\Omega$, $C = 10\ \mu F$. The input voltage is sinusoidal having frequency of 50 Hz and rms value of 10 V. Under ideal condition the phase of i_s with respect to V_s ____.



Q.43 Consider the ideal op-amp circuit shown below.

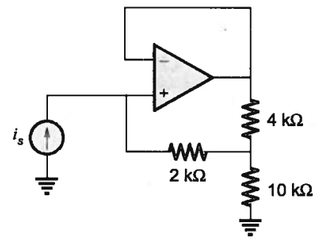


If it is given that

$$\frac{R_2}{R_1} = 10, \frac{R_4}{R_3} = 11$$

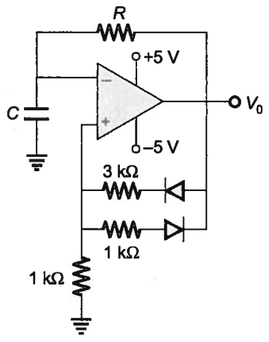
then the common mode rejection ratio (CMRR) is _____ dB.

Q.44 For the circuit shown below the input resistance is _____ kΩ.



Q.45 An op-amp has an open-loop gain of 10^5 and an open-loop upper cut-off frequency of 10 Hz. If this op-amp is connected as an amplifier with a closed-loop gain of 100, then the new upper cut-off frequency is _____ kHz.

Q.46 An oscillator circuit using ideal op-amp and diodes is shown in the figure.

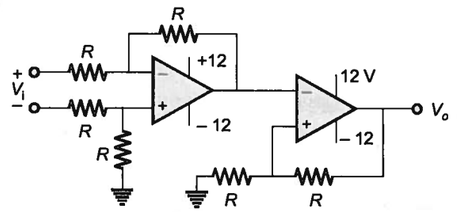


The time duration for +ve part of the cycle is Δt_1 and for –ve part is Δt_2. The value of $e^{\frac{\Delta t_1 - \Delta t_2}{RC}}$ will be _____ .

[GATE-2014]

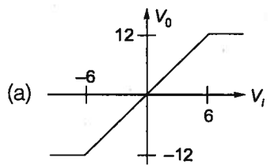
Try Yourself

T1. For the circuit shown below

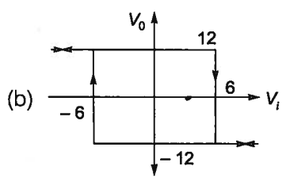


the transfer characteristic can be represented as

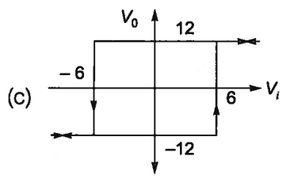
(a)



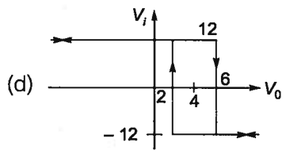
(b)



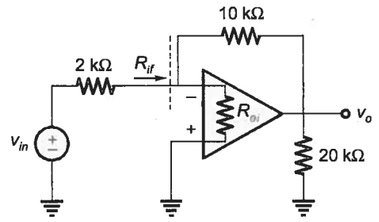
(c)



(d)

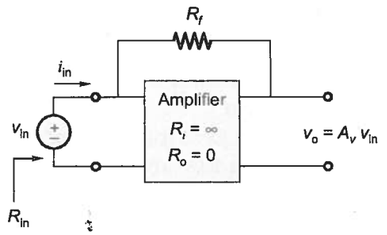


T2. Consider an op-amp circuit shown in figure, with an open loop gain of $A_{ol} = 10^5$ and open loop input impedance $R_{oi} = 10$ kΩ. If the output resistance of op-amp is zero, than closed loop input impedance (R_{if}) at the inverting terminal of op-amp is



(a) $R_{if} = 10$ kΩ (b) $R_{if} = 1$ kΩ
(c) $R_{if} = 40$ kΩ (d) $R_{if} = 0.1$ Ω

T3. Consider the amplifier circuit shown below, where A_v is the voltage gain of amplifier.

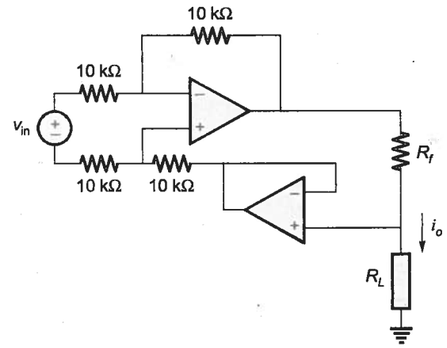


What is the value of input resistance, $R_{in} = \frac{v_{in}}{i_{in}}$?

(a) $\frac{A_v R_f}{1 - A_v}$ (b) $(1 - A_v) R_f$

(c) $\frac{R_f}{1 - A_v}$ (d) $\frac{(1 - A_v)}{A_v} R_f$

T4. Consider the circuit shown in figure below. Assume op-amp is ideal.

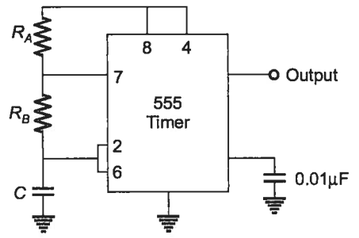


What is the value of current i_o?

(a) $-\frac{v_{in}}{10\text{ k}\Omega}$ (b) $-\frac{v_{in}}{R_f}$

(c) $-\frac{v_{in}}{R_L}$ (d) None of the above

T5. In the figure shown below.



If $R_A = R_B$ then

(a) Duty cycle of the output wave is greater than 50%.
(b) Duty cycle of the output wave is 50%.
(c) R_A and R_B do not influence the duty cycle of the output.
(d) Duty cycle is 50% irrespective of R_A and R_B values.