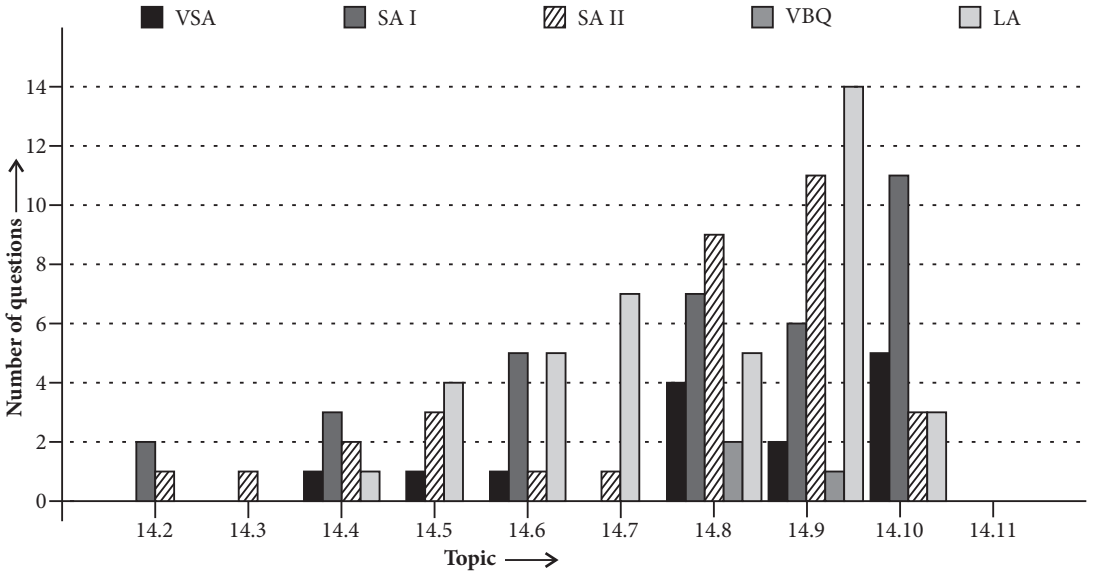
14 Semiconductor Electronics: Materials, Devices and Simple Circuits

Topicwise Analysis of Last 10 Years' CBSE Board Questions



- Maximum weightage is of *Junction Transistor.*
- Maximum VSA and SA I type questions were asked from *Digital Electronics and Logic Gates.*
- Maximum SA II and LA type questions were asked from *Junction Transistor.*

QUICK RECAP

Classification of solids on the basis of their conductivity : On the basis of the relative values of electrical conductivity (σ) and resistivity ($\rho = 1/\sigma$), the solids are broadly classified as,

- **Metals** : Those solids which have high conductivity and very low resistivity. The value

of conductivity for metals lies in between 10^2 to 10^8 S m^{-1} and of resistivity in between 10^{-2} to 10^{-8} Ω m.

- **Insulators** : Those solids which have low conductivity and high resistivity. The value of conductivity for insulators lies between 10^{-11} to 10^{-19} S m^{-1} and of resistivity between 10^{11} to 10^{19} Ω m.
- **Semiconductors** : Those solids which have conductivity and resistivity intermediate to metals and insulators. The value of conductivity for semiconductors lies in between 10^5 to 10^{-6} S m^{-1} and of resistivity between 10^{-5} to 10^6 Ω m.

Energy bands of solids or band theory of solids

- **Valence band :** This band contains valence electrons. This band may be partially or completely filled with electrons. This band is never empty. Electrons in this band do not contribute to electric current.
- **Conduction band :** In this band, electrons are rarely present. This band is either empty or partially filled. Electrons in the conduction band are known as free electrons. These electrons contribute to the electric current.
- **Forbidden energy gap or forbidden band :** The energy gap between the valence band and conduction band is known as forbidden energy gap or forbidden band. No electrons are present in this gap. It is a measure of energy band gap.
  - The minimum energy required for shifting electrons from valence band to conduction band is known as energy band gap.
  - If λ is the wavelength of radiation used in shifting the electron from valence band to conduction band, then energy band gap is

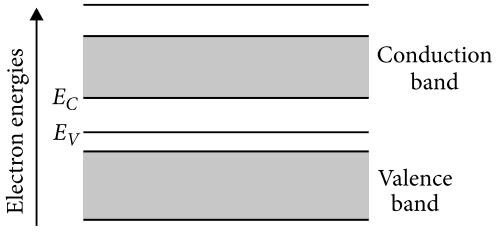
$$E_g = h\upsilon = \frac{hc}{\lambda}$$

where h is called Planck's constant and c is the speed of light.

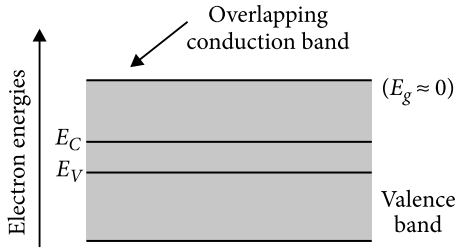
  - The forbidden energy gap E_g in a semiconductor depends upon temperature.
  - Fermi energy : It is the maximum possible energy possessed by free electrons of a material at absolute zero temperature (*i.e.* 0 K)

Differences between metals, insulators and semiconductors on the basis of band theory

- **Metals**
  - In metals either the conduction band is partially filled or conduction band and valence band partially overlap each other.
  - In metals, there is no forbidden energy gap between the valence and conduction bands.

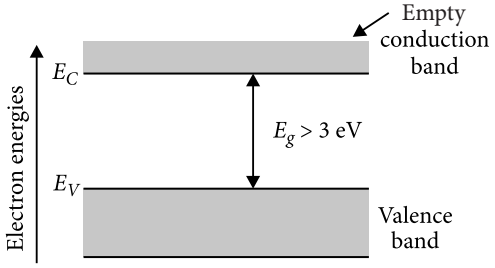


(i)

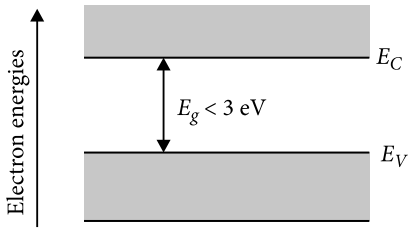


(ii)

- **Insulators**
  - In insulators, valence band is completely filled and conduction band is completely empty.
  - In insulators, there is a very wide forbidden energy gap between the valence and conduction bands. It is of the order of 5 eV or more.



- **Semiconductors**
  - In semiconductors, valence band is completely filled and the conduction band is empty.
  - In semiconductors, there is a small forbidden energy gap between the valence and the conduction bands. It is of the order of 1 eV. For silicon, it is 1.1 eV and for germanium it is 0.72 eV.



- At absolute zero, semiconductors behave as a perfect insulator.
- Hole : It is a seat of positive charge which is produced when an electron breaks away from a covalent bond in a semiconductor. Hole has a positive charge equal to that of electron. Mobility of hole is smaller than that of electron.

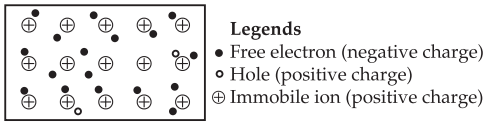
Intrinsic semiconductor : A pure semiconductor which is free from every impurity is known as intrinsic semiconductor. Germanium (Ge) and silicon (Si) are the important examples of intrinsic semiconductors.

- In intrinsic semiconductor, $n_e = n_h = n_i$ where n_e, n_h are number density of electrons in conduction band and number density of holes in valence band, n_i is the intrinsic carrier concentration.
- When an electric field is applied across an intrinsic semiconductor, electrons and holes move in opposite directions so that total current (I) through the pure semiconductor is given by $I = I_e + I_h$ where I_e is the free electron current and I_h is the hole current.
- **Effect of temperature on conductivity of intrinsic semiconductor**
  - An intrinsic semiconductor will behave as a perfect insulator at absolute zero.
  - With increasing temperature, the density of hole-electron pairs increases and hence the conductivity of an intrinsic semiconductor increases with increase in temperature. In other words, the resistivity (inverse of conductivity) decreases as the temperature increases.
  - The semiconductors have negative temperature coefficient of resistance.

Doping : It is a process of deliberate addition of a desirable impurity to a pure semiconductor in order to increase its conductivity. The impurity atoms added are known as dopants.

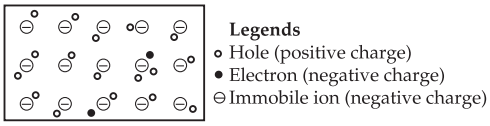
Extrinsic semiconductor : A doped semiconductor is known as extrinsic semiconductor. Extrinsic semiconductors are of two types :

- ***n*-type semiconductor**
  - When a pure semiconductor of Si or Ge (tetravalent) is doped with a group V pentavalent impurities like arsenic (As), antimony (Sb), phosphorus (P) etc, we obtain a *n*-type semiconductor. The pentavalent impurity atoms are known as donor atoms.
  - It is called *n*-type semiconductor because the conduction of electricity in such semiconductor is due to motion of electrons *i.e.* negative charges.
  - It is called donor type semiconductor, because the doped impurity atom donates one free electron to semiconductor for conduction.
  - In *n*-type semiconductor electrons are majority carriers and holes are minority carriers.
  - The representation of *n*-type semiconductor is as shown in the figure.



  - *n*-type semiconductor is neutral.
  - In *n*-type semiconductor $n_e \approx N_d >> n_h$ where N_d is the density of donor atoms.
- ***p*-type semiconductor :** When a pure semiconductor of Si or Ge (tetravalent) is doped with a group III trivalent impurities like aluminium (Al), boron (B), indium (In) etc, we obtain a *p*-type semiconductor. The trivalent impurity atoms are known as acceptor atoms.
  - It is called *p*-type because the conduction of electricity in such semiconductor is due to motion of holes *i.e.* positive charges.

- It is called acceptor type semiconductor because the doped impurity atom creates a hole in semiconductor which accepts the electron, resulting conduction in *p*-type semiconductor.
- In *p*-type semiconductor, holes are majority carriers and electrons are minority carriers.
- The representation of *p*-type semiconductor is as shown in the figure.



- *p*-type semiconductor is neutral.
- In *p*-type semiconductor

$n_h \approx N_a >> n_e$

where N_a is the density of acceptor atoms.

Mass action law : Under thermal equilibrium, the product of the free negative and positive concentrations is a constant independent of the amount of donor and acceptor impurity doping. This relationship is known as the mass action law and is given by

$$n_e n_h = n_i^2$$

where n_e, n_h are the number density of electrons and holes respectively and n_i is the intrinsic carriers concentration.

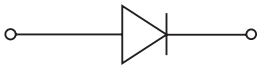
Electrical conductivity in semiconductor : The conductivity of the semiconductor is given by

$\sigma = e(n_e\mu_e + n_h\mu_h)$

where μ_e and μ_h are the electron and hole mobilities, n_e and n_h are the electron and hole densities, e is the electronic charge.

- The conductivity of an intrinsic semiconductor is $\sigma_i = n_i e(\mu_e + \mu_h)$
- The conductivity of *n*-type semiconductor is $\sigma_n = eN_d\mu_e$
- The conductivity of *p*-type semiconductor is $\sigma_p = eN_a\mu_h$

***p-n* junction :** When donor impurities are introduced into one side and acceptors into the other side of a single crystal of an intrinsic semiconductor, a *p-n* junction is formed. It is also known as junction diode. The most important characteristic of a *p-n* junction is its ability to conduct current in one direction only. In the other (reverse) direction it offers very high resistance. It is symbolically represented by



Depletion region : In the vicinity of junction, the region containing the uncompensated acceptor and donor ions is known as depletion region. There is a depletion of mobile charges (holes and free electrons) in this region. Since this region has immobile (fixed) ions which are electrically charged it is also known as the space charge region. The electric field between the acceptor and the donor ions is known as a barrier. The physical distance from one side of the barrier to the other is known as the width of the barrier. The difference of potential from one side of the barrier to the other side is known as the height of the barrier.

- For a silicon *p-n* junction, the barrier potential is about 0.7 V, whereas for a germanium *p-n* junction it is approximately 0.3 V.
- The width of the depletion layer and magnitude of potential barrier depend upon the nature of the material of semiconductor and the concentration of impurity atoms. The thickness of the depletion region is of the order of one tenth of a micrometre.

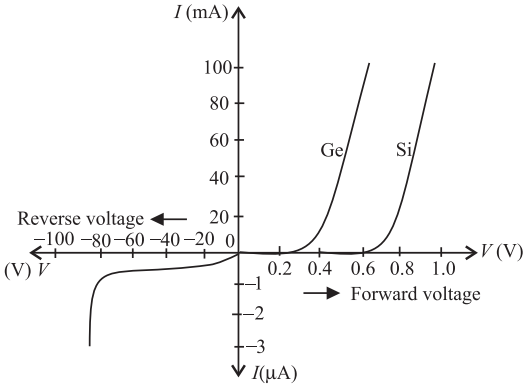
Forward biasing of a *p-n* junction : When the positive terminal of external battery is connected to *p*-side and negative to *n*-side of *p-n* junction, then the *p-n* junction is said to be forward biased.

- In forward biasing, the width of the depletion region decreases and barrier height reduces.
- The resistance of the *p-n* junction becomes low in forward biasing.

Reverse biasing of a *p-n* junction : When the positive terminal of the external battery is connected to *n*-side and the negative terminal to *p*-side of a *p-n* junction, then the *p-n* junction is said to be reverse biased.

- In reverse biasing, the width of the depletion region increases and barrier height increases.
- The resistance of the *p-n* junction becomes high in reverse biasing.

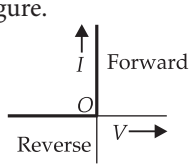
- **Breakdown voltage :** A very small current flows through *p-n* junction, when it is reverse biased. The flow of the current is due to the movement of minority charge carriers. The reverse current is almost independent of the applied voltage. However, if the reverse bias voltage is continuously increased, for a certain reverse voltage, the current through the *p-n* junction will increase abruptly. This reverse bias voltage is thus known as breakdown voltage. There can be two different causes for the break down. One is known as zener breakdown and the other is known as avalanche breakdown.
- ***I-V* characteristics of a *p-n* junction :** The *I-V* characteristics of a *p-n* junction do not obey Ohm's law. The *I-V* characteristics of a *p-n* junction are as shown in the figure.



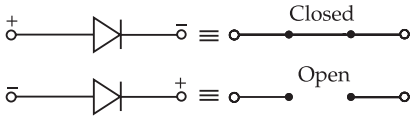
  - **Knee voltage :** In forward biasing, the voltage at which the current starts to increase rapidly is known as cut-in or knee voltage. For germanium it is 0.3 V while for silicon it is 0.7 V.
  - **Dynamic resistance :** It is defined as the ratio of a small change in voltage (ΔV) applied across the *p-n* junction to a small change in current ΔI through the junction.

$$r_d = \frac{\Delta V}{\Delta I}$$

Ideal diode: A diode permits only unidirectional conduction. It conducts well in the forward direction and poorly in the reverse direction. It would have been ideal if a diode acts as a perfect conductor (with zero voltage across it) when it is forward biased, and as a perfect insulator (with no current flows through it) when it is reverse biased. The *I-V* characteristics of an ideal diode as shown in figure.

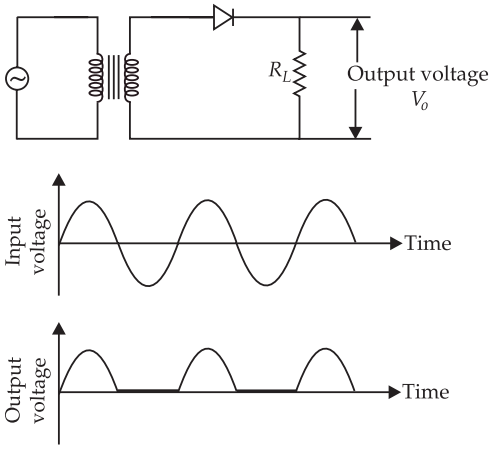


- An ideal diode acts like an automatic switch.
- In forward bias, it acts as a closed switch whereas in reverse bias it acts as an open switch as shown in the figure

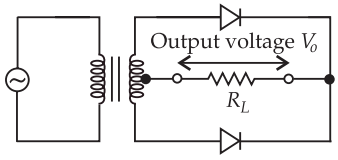


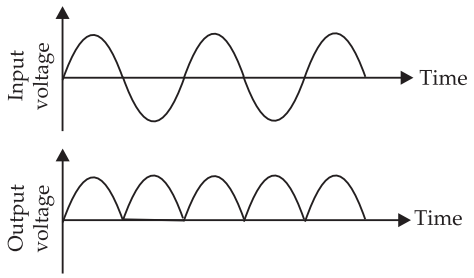
Rectifier : It is a device which converts ac voltage to dc voltage. Diode is used as a rectifier. Rectifier is based on the fact that, a forward bias *p-n* junction conducts and a reverse bias *p-n* junction does not conduct.

- **Half wave rectifier :** Diode conducts corresponding to positive half cycle and does not conduct during negative half cycle. Hence, *AC* is converted by diode into undirectional pulsating *DC*. This action is known as half-wave rectification.



- **Full wave rectifier :** The circuit diagram, input and output waveforms for a full wave rectifier are as shown in the figure.





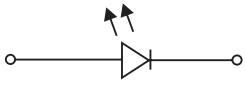
- **Ripple factor :** The ripple factor is a measure of purity of the dc output of a rectifier, and is defined as

$$r = \frac{\text{rms value of the components of wave}}{\text{average or dc value}}$$

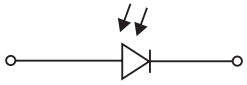
$$r = \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1}$$

Special Purpose *p-n* Junction Diodes :

- **Light emitting diode (LED) :** It converts electrical energy into light energy. It is a heavily doped *p-n* junction which operates under forward bias and emits spontaneous radiation.
  - The *I-V* characteristics of a LED is similar to that of Si junction diode. But the threshold voltages are much higher and slightly different for each colour. The reverse breakdown voltages of LEDs are very low, typically around 5 V.
  - The semiconductor used for fabrication of visible LEDs must at least have a band gap of 1.8 eV. The compound semiconductor gallium arsenide phosphide (GaAsP) is used for making LEDs of different colours. GaAs is used for making infrared LED.
  - The symbol of a LED is shown in the figure.

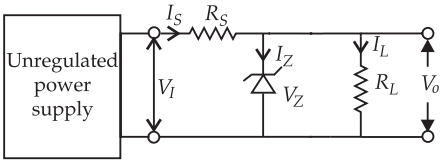


- **Photodiode :** A photodiode is a special type *p-n* junction diode fabricated with a transparent window to allow light to fall on the diode. It is operated under reverse bias. When it is illuminated with light of photon energy greater than the energy gap of the semiconductor, electron-hole pairs are generated in near depletion region.
  - The symbol of a photodiode is shown in the figure below.



- **Solar cell :** It converts solar energy into electrical energy. A solar cell is basically a *p-n* junction which generates emf when solar radiation falls on the *p-n* junction. It works on the same principle (photovoltaic effect) as the photodiode, except that no external bias is applied and the junction area is kept large.
- **Zener diode :** It was invented by *C.* Zener. It is designed to operate under reverse bias in the breakdown region and is used as a voltage regulator. The symbol for Zener diode is shown in the figure.

  - **Zener diode as a voltage regulator :** The circuit diagram for zener diode as a voltage regulator is shown in the figure below.



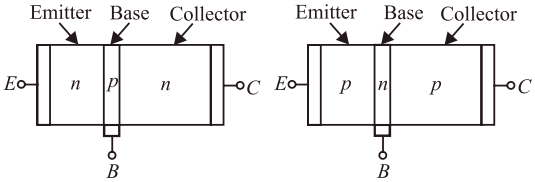
Transistor : A junction transistor is a three terminal semiconductor device consisting of *p-n* junctions formed by placing a thin layer of doped semiconductor (*p*. type or *n*-type) between two similar layers of opposite type.

There are two types of transistor :

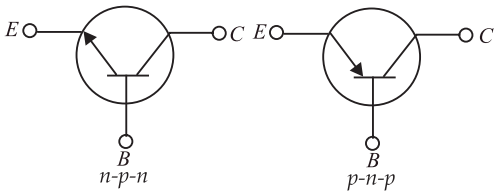
(i) *p-n-p* transistor : Here, two segments of *n*-type semiconductor (emitter and collector) are separated by a segment of *p*-type semiconductor (base).

(ii) *p-n-p* transistor : Here two segments of *p*-type (termed as emitter and collector) are separated by a segment of *n*-type semiconductor (base).

- The schematic representations of a *n-p-n* and *p-n-p* transistors are shown in the figure.

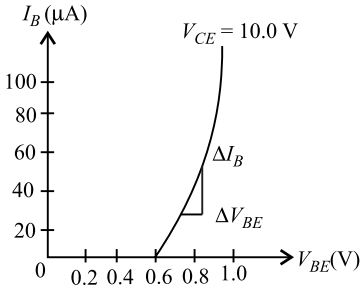


- The symbols for *n-p-n* and *p-n-p* transistors are shown in the figure below.



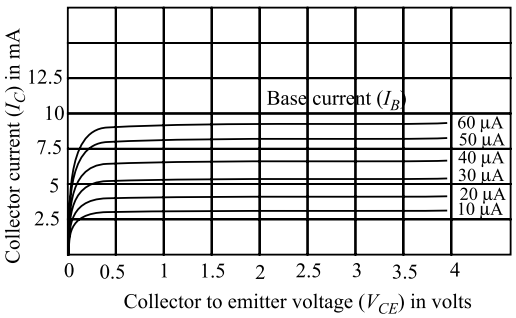
- In operation of a transistor, $I_E = I_B + I_C$ where I_E is emitter current, I_B is base current, I_C is the collector current.
- A transistor can be operated in any one of the following three configurations :
  - Common emitter (*CE*)
  - Common base (*CB*)
  - Common collector (*CC*)
- **Input characteristics of a transistor**

The variation of the input current with the input voltage for a given output voltage is known as input characteristics of a transistor.

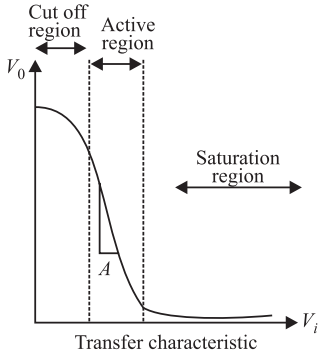


- **Output characteristics of a transistor**

The variation of the output current with the output voltage for a given input current is known as output characteristics of a transistor.

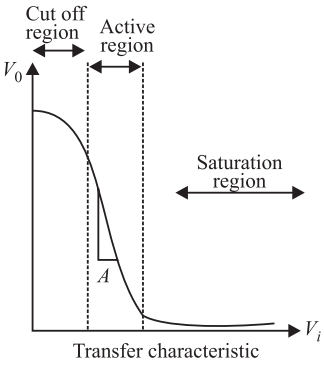


Transistor as a switch :



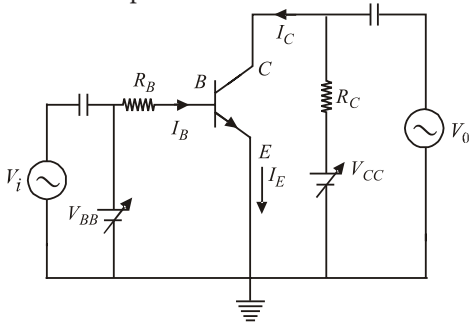
When the transistor is used in the cut off region or saturation region, it acts as a switch.

Transistor as an amplifier :



When the transistor is used in the active region, it acts as an amplifier.

Common emitter amplifier : In the common emitter transistor amplifier, the input signal voltage and the output collector voltage are 180° out of phase.



CE amplifier with transistor

- **dc current gain :** It is defined as the ratio of the collector current (I_C) to the base current (I_B).

$$\beta_{dc} = \frac{I_C}{I_B}$$

- **ac current gain :** It is defined as ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B).

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

- **Voltage gain :** It is defined as the ratio of output voltage to the input voltage.

$$A_v = \frac{V_o}{V_i} = -\beta_{ac} \times \frac{R_o}{R_i}$$

where R_o and R_i are the output and input resistances.

Negative sign represents that output voltage is opposite in phase with the input voltage.

- **Power gain :** It is defined as the ratio of the output power to the input power.

$$A_p = \frac{\text{output power } (P_o)}{\text{input power } (P_i)} = \beta_{ac} \times A_v$$

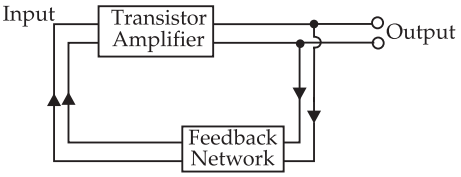
Note : Voltage gain (in dB) $= 20 \log_{10} \frac{V_o}{V_i}$

$= 20 \log_{10} A_v$

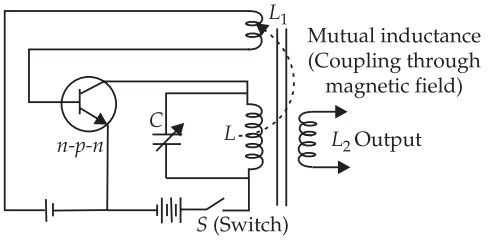
Power gain (in dB) $= 10 \log \frac{P_o}{P_i}$

Transistor as an oscillator : An oscillator generates ac output signal without any input ac signal. An oscillator is a self sustained amplifier in which a part of output is fed back to the input in the same phase (this process is called positive feedback).

- The block diagram of an oscillator is shown in the figure.



- The circuit diagram of the tuned collector oscillator is shown in the figure below.



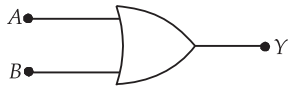
- The frequency of the oscillation is given by

$$\upsilon = \frac{1}{2\pi\sqrt{LC}}$$

Logic gates : A digital circuit with one or more input signals but only one output signal is known as logic gate.

There are three basic logic gates :

- **OR gate :** An OR gate has two or more inputs but only one output.
  - The logic symbol of OR gate is

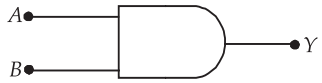


  - The truth table for OR gate is

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

  - The Boolean expression for OR gate is $Y = A + B$

- **AND gate :** An AND gate has two or more inputs but only one output.
  - The logic symbol of AND gate is

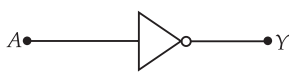


  - The truth table for AND gate is

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

  - The Boolean expression for AND gate is $Y = A \cdot B$

- **NOT gate :** The NOT gate is the simplest of all logic gates. It has only one input and one output.
  - The logic symbol of NOT gate is



  - The truth table for NOT gate is

Input	Output
A	Y
0	1
1	0

– The Boolean expression for NOT gate is $Y = \overline{A}$

▶ **NAND gate :** It is an AND gate followed by a NOT gate.

– The logic symbol for NAND gate is

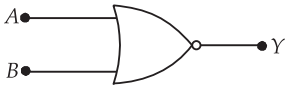
– The truth table for NAND gate is

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

– The Boolean expression for NAND gate is $Y = \overline{A \cdot B}$

▶ **NOR gate :** It is an OR gate followed by a NOT gate.

– The logic symbol of NOR gate is



– The truth table for NOR gate is

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

– The Boolean expression for NOR gate is $Y = \overline{A + B}$

Previous Years' CBSE Board Questions

14.2 Classification of Metals, Conductors & Semiconductors

SA I (2 marks)

1. Distinguish between a metal and an insulator on the basis of energy band diagrams.
(Foreign 2014)

2. Draw a plot showing the variation of resistivity of a (i) conductor and (ii) semiconductor, with the increase in temperature.
(2/3, Delhi 2014C)

SA II (3 marks)

3. Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams. *(AI 2014)*

14.3 Intrinsic Semiconductor

SA II (3 marks)

4. Explain the formation of energy bands in solids. Draw energy band diagrams for (i) a conductor, (ii) an intrinsic semiconductor. *(AI 2007)*

14.4 Extrinsic Semiconductor

VSA (1 mark)

5. What is the difference between an *n*-type and a *p*-type extrinsic semiconductor? *(Delhi 2012C)*

SA I (2 marks)

6. Distinguish between 'intrinsic' and 'extrinsic' semiconductors. *(Delhi 2015)*

7. Draw energy band diagrams of an *n*-type and *p*-type semiconductor at temperature $T > 0$ *K*. Mark the donor and acceptor energy levels with their energies.
(Foreign 2014)

8. Write two characteristic features to distinguish between *n*-type and *p*-type semiconductors.
(Foreign 2012)

SA II (3 marks)

9. (i) Distinguish between *n*-type and *p*-type semiconductors on the basis of energy band diagrams.

(ii) Compare their conductivities at absolute zero temperature and at room temperature.
(Delhi 2015C)

10. Draw the energy band diagrams of
(i) *n*-type and
(ii) *p*-type semiconductor at temperature, $T > 0$K.
In the case *n*-type Si semiconductor, the donor energy level is slightly below the bottom of conduction band whereas in *p*-type semiconductor, the acceptor energy level is slightly above the top of the valence band. Explain, what role do these energy levels play in conduction and valence bands. *(AI 2015C)*

LA (5 marks)

11. Distinguish between an intrinsic semiconductor and a *p*-type semiconductor. Give reason why a *p*-type semiconductor is electrically neutral, although $n_h >> n_e$. *(2/5, Foreign 2013)*

14.5 *p-n* Junction

VSA (1 mark)

12. Why can't we take one slab of *p*-type semiconductor and physically it to another slab of *n*-type semiconductor to get *p-n* junction?
(AI 2010C)

SA II (3 marks)

13. Explain with the help of the diagram the formation of depletion region and barrier potential in a *p-n* junction. *(2/3, AI 2016)*

14. Write briefly the important processes that occur during the formation of *p-n* junction. With the help of necessary diagrams, explain the term barrier potential. *(Foreign 2015)*

15 Name the important process that occur during the formation of a *p-n* junction. Explain briefly,

with the help of a suitable diagram, how a *p-n* junction is formed. Define the term 'barrier potential'. *(Foreign 2011)*

LA (5 marks)

16. State briefly the processes involved in the formation of *p-n* junction explaining clearly how the depletion region is formed. *(2/5, Delhi 2014)*

17. Explain with the help of diagram, how a depletion layer and barrier potential are formed in a junction diode. *(3/5, Delhi 2014C)*

18. Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a *p-n* junction. *(2/5, AI 2012)*

19. Explain the formation of depletion layer and barrier potential in *p-n* junction. *(2/5, Delhi 2010)*

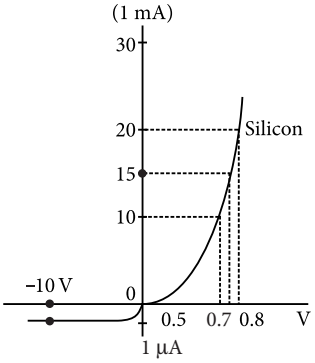
14.6 Semiconductor Diode

VSA (1 mark)

20. What happens to the width of depletion layer of a *p-n* junction when it is (i) forward biased, (ii) reverse biased? *(AI 2011)*

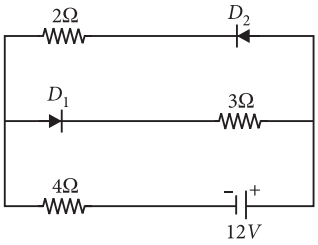
SA I (2 marks)

21. The *V-I* characteristic of a silicon diode is as shown in the figure. Calculate the resistance of the diode at (i) $I = 15$ mA and (ii) $V = -10$ V



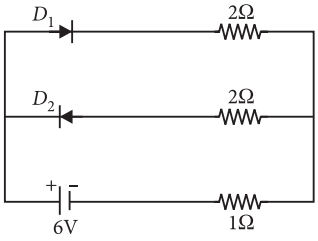
(Foreign 2015)

22. The circuit shown in the figure has two oppositely connected ideal diodes connected in parallel. Find the current flowing through each diode in the circuit.



(Foreign 2013)

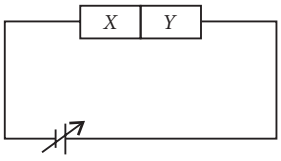
23. Assuming that the two diodes D_1 and D_2 used in the electric circuit shown in the figure are ideal, find out the value of the current flowing through 1 Ω resistor.



(Delhi 2013C)

24. Draw the circuit diagrams showing how a *p-n* junction diode is (i) forward biased and (ii) reverse biased. How is the width of layer affected in the two cases? *(AI 2011C)*

25. Two semiconductor material *X* and *Y* shown in the given figure are made by doping germanium crystal with indium and arsenic respectively. The two are joined end to end and connected to a battery as shown.



(i) Will the junction be forward biased or reverse biased ?

(ii) Sketch a *V-I* graph for this arrangement. *(AI 2007)*

SA II (3 marks)

26. Draw *V-I* characteristics of a *p-n* junction diode. Answer the following questions, giving reasons.

(i) Why is the current under reverse bias almost independent of the applied potential upto a critical voltage?

(ii) Why does the reverse current show a sudden increase at the critical voltage?
Name any semiconductor device which operates under the reverse bias in the breakdown region. *(AI 2013)*

LA (5 marks)

27. Using the necessary circuit diagrams, show how the *V-I* characteristics of a *p-n* junction are obtained in
(i) Forward biasing
(ii) Reverse biasing *(Delhi 2014)*

28. Draw the circuit arrangement for studying the *V-I* characteristics of a *p-n* junction diode in (i) forward and (ii) reverse bias. Briefly explain how the typical *V-I* characteristics of a diode are obtained and draw these characteristics.
(AI 2014C)

29. Explain, how the heavy doping of both *p* and *n*-side of a *p-n* junction diode results in the electric field of the junction being extremely high even with a reverse bias voltage of a few volts. *(2/5, Foreign 2013)*

30. Define the terms 'depletion layer' and 'barrier potential' for a *p-n* junction. How does (i) an increase in the doping concentration and (ii) biasing across the junction, affect the width of the depletion layer? *(3/5 AI 2013C)*

31. Explain the formation of depletion region for *p-n* junction diode. How does the width of this region change when the junction is (i) forward biased, (ii) reverse biased?
(2/5, AI 2012C)

32. Draw the circuit diagrams of a *p-n* junction diode in (i) forward bias, (ii) reverse bias. How are these circuits used to study the *V–I* characteristics of a silicon diode? Draw the typical *V–I* characteristics. *(3/5, AI 2010)*

14.7 Application of junction diode as a rectifier

SA II (3 marks)

33. Draw the circuit diagram of a half wave rectifier and explain its working. *(1/3, AI 2016)*

LA (5 marks)

34. Explain briefly, with the help of circuit diagram, the working of a full wave rectifier. Draw its input and output waveforms. *(Delhi 2015C)*

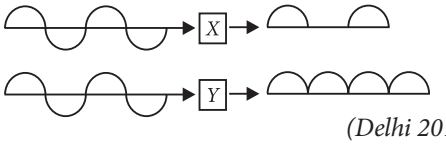
35. (i) With the help of a labelled circuit diagram, explain how a junction diode is used as a full wave rectifier. Draw its input, output wave-forms.
(ii) How do you obtain steady d.c. output from the pulsating voltage? *(4/5, Delhi 2013C)*

36. Draw the circuit diagram of a *p-n* diode used as a half-wave rectifier. Explain its working.
(AI 2013C)

37. Draw the circuit diagram of a full wave rectifier using *p-n* junction diode. Explain its working and show the output, input waveforms.
(3/5, AI 2012C)

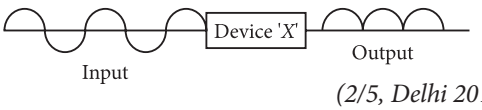
38. Draw the circuit diagram of a full wave rectifier. Briefly explain its working. *(3/5, AI 2012C)*

39. An a.c. signal is fed into two circuits '*X*' and '*Y*' and the corresponding output in the two cases have the waveforms as shown.
(a) Identify the circuits '*X*' and '*Y*'. Draw their labelled circuit diagrams.
(b) Briefly explain the working of circuit *Y*.
(c) How does the output waveform from circuit *Y* get modified when a capacitor is connected across the output terminals parallel to the load resistor?



(Delhi 2011C)

40. In the figure given below the input waveform is converted into the output waveform by a device 'X'. Name the device and draw its circuit diagram.



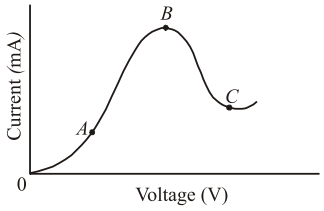
(2/5, Delhi 2010)

41. Sate the principle of working of *p-n* diode as a rectifier. Explain, with the help of a circuit diagram, the use of *p-n* diode as a full wave rectifier. Draw a sketch of the input and output waveforms. *(Delhi 2007)*

14.8 Special purpose *p-n* junction diodes

VSA (1 mark)

42. The graph shown in the figure represents a plot of current versus voltage for a given semiconductor. Identify the region, if any, over which the semiconductor has a negative resistance.

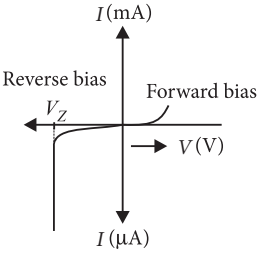


(AI 2013)

43. What is the function of a photodiode?

(AI 2013C)

44. Figure shows the *V-I* characteristic of a given device. Name the device and write where it is used. *(Delhi 2010C)*



45. State the reason, why GaAs is most commonly used in making of a solar cell. *(AI 2008)*

SA I (2 marks)

46. Explain, with the help of a circuit diagram, the working of a photodiode. Write briefly how it is used to detect the optical signals. *(Delhi 2013)*

47. (a) Mention the important considerations required while fabricating a *p-n* junction diode to be used as a light emitting diode (LED).
(b) What should be the order of band gap of an LED if it is required to emit light in the visible range? *(Delhi 2013C)*

48. The current in the forward bias is known to be more (~mA) than the current in the reverse bias (~ μA). What is the reason, then, to operate the photodiode in reverse bias? *(Delhi 2012)*

49. How does a light emitting diode (LED) work? Give two advantages of LED's over the conventional incandescent lamps. *(Foreign 2012)*

50. (a) Why are Si and GaAS preferred materials for fabrication in solar cells?
(b) Draw *V-I* characteristic of solar cell and mention its significance. *(AI 2012C)*

51. Name the semiconductor device that can be used to regulate an unregulated dc power supply. With the help of *V-I* characteristics of this device, explain its working principle. *(Delhi 2011)*

52. Draw the circuit diagram of an illuminated photodiode in reverse bias. How is photodiode used to measure light intensity? *(Delhi 2010)*

SA II (3 marks)

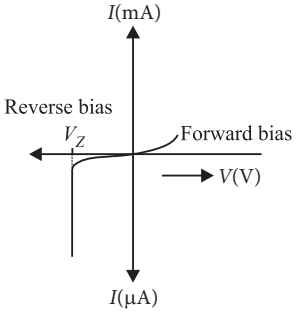
53. (i) Describe the working principle of a solar cell. Mention three basic processes involved in the generation of emf.
(ii) Why are Si and GaAs preferred materials for solar cells? *(Foreign 2016)*

54. With what considerations in view, a photodiode is fabricated? State its working with the help of a suitable diagram.
Even though the current in the forward bias is known to be more than in the reverse bias, yet the photodiode works in reverse bias. What is the reason? *(Delhi 2015)*

55. (a) Why is zener diode fabricated by heavily doping both *p*- and *n*-sides of the junction?
(b) Draw the circuit diagram of zener diode as a voltage regulator and briefly explain its working. *(Foreign 2014)*

56. (a) How is a photodiode fabricated?
(b) Briefly explain its working. Draw its *V-I* characteristics for two different intensities of illumination. *(Foreign 2014)*

57. (i) The figure shows the *V-I* characteristics of a semiconductor device. Identify this device.
(ii) Explain briefly, using the necessary circuit diagram, how this device is used as a voltage regulator.



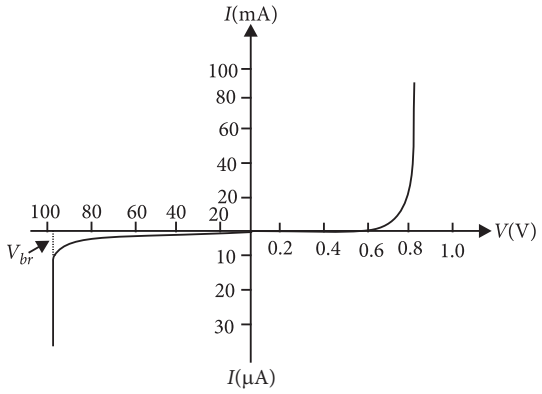
(Delhi 2012C)

58. The given figure below shows the *V-I* characteristic of a semiconductor diode.

(i) Identify the semiconductor diode used.

(ii) Draw the circuit diagram to obtain the given characteristic of this device.

(iii) Briefly explain how this diode can be used as a voltage regulator.



(AI 2011)

59. (a) Describe briefly with the help of a necessary circuit diagram, the working principle of a solar cell.

(b) Why are Si and GaAs preferred materials for solar cells? Explain.

(AI 2011C)

60. Draw a circuit diagram of LED. What are its advantages? *(2/3, Delhi 2008)*

61. Explain, with the help of a schematic diagram, the principle and working of a light emitting diode. What criterion is kept in mind while choosing the semiconductor material for such a device? Write any two advantages of light emitting diode over conventional incandescent lamps. *(Delhi 2007)*

VBQ (4 marks)

62. Meeta's father was driving her to the school. At the traffic signal she noticed that each traffic light was made of many tiny lights instead of a single bulb. When Meeta asked this question to her father, he explained the reason for this.

Answer the following questions based on above information :

(i) What were the values displayed by Meeta and her father ?

(ii) What answer did Meeta's father give ?

(iii) What are the tiny lights in traffic signals called and how do these operate ?

(Delhi 2016)

63. Ameen had been getting huge electricity bill for the past few months. He was upset about this. One day his friend Rohit, an electrical engineer by profession, visited his house. When he pointed out his anxiety about this to Rohit, his friend found that Ameen was using traditional incandescent lamps and using old fashioned air conditioner. In addition there was no proper earthing in the house. Rohit advised him to use CFL bulbs of 28 W instead of 1000W – 200V and also advised him to get proper earthing in the house. He made some useful suggestion and asked him to spread this message to his friends also.

(i) What qualities/values, in your opinion did Rohit possess?

(ii) Why CFLs and LEDs are better than traditional incandescent lamps?

(iii) In what way earthing reduces electricity bill? *(Delhi 2015C)*

LA (5 marks)

64. (a) Why is a zener diode considered as a special purpose semiconductor diode?

(b) Draw the *V-I* characteristic of a zener diode and explain briefly how reverse current suddenly increases at the breakdown voltage.

(c) Describe briefly with the help of a circuit diagram how a zener diode works to obtain a constant d.c. voltage from the unregulated d.c. output of a rectifier. *(Foreign 2012)*

65. Name the device which is used as a voltage regulator. Draw the necessary circuit diagram and explain its working. *(2/5, AI 2012)*

66. What is a light emitting diode (LED)? Mention two important advantages of LEDs over conventional lamps. *(2/5, AI 2010)*

67. (a) Draw *V-I* characteristics of a Zener diode.
(b) Explain with the help of a circuit diagram, the use of a zener diode as a voltage-regulator.
(c) A photoiode is operated under reverse bias although in the forward bias the current is known to be more than the current in the reverse bias. Explain giving reason.
(Foreign 2010)

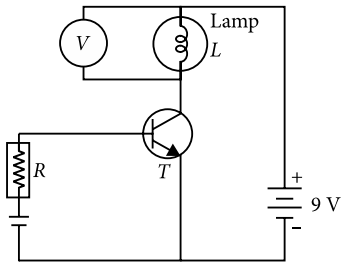
68. State the main practical applications of LED. Explain, giving reason, why semiconductor used for fabrication of visible light LEDs must have a band of at least (nearly) 1.8 eV.
(2/5, Delhi 2010C)

14.9 Junction Transistor

VSA (1 mark)

69. In a transistor, doping level in base is increased slightly. How will it affect (i) collector current and (ii) base current? *(Delhi 2011)*

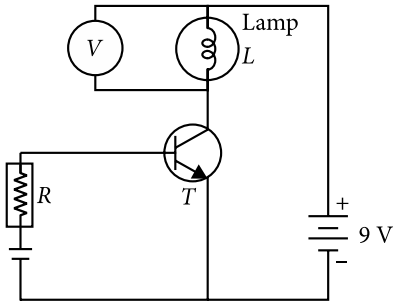
70. In the given circuit, a voltmeter '*V*' is connected across lamp '*L*'. What changes would you observe in the lamp '*L*' and the voltmeter, if the value of resistor '*R*' is reduced?



(Delhi 2011C)

SA I (2 marks)

71. In the given circuit diagram a voltmeter '*V*' is connected across a lamp '*L*'. How would (i) the brightness of the lamp and (ii) voltmeter reading '*V*' be affected, if the value of resistance '*R*' is decreased? Justify your answer.



(Delhi 2013)

72. Draw typical output characteristics of an *n-p-n* transistor in CE configuration. Show how these characteristics can be used to determine output resistance. *(AI 2013)*

73. Describe briefly with the help of a circuit diagram, how the flow of current carriers in a *p-n-p* transistor is regulated with emitter-base junction forward biased and base-collector junction reverse biased. *(AI 2012)*

74. Draw the transfer characteristic curve of a base biased transistor in CE configuration.
Explain clearly how the active region of the V_o versus V_i curve in a transistor is used as an amplifier. *(Delhi 2011)*

75. Define the following terms :
(i) Input resistance r_i
(ii) Current amplication factor β of a transistor used in its CE configuration. *(AI 2010C)*

76. (i) A transistor has a current gain of 30. If the collector resistance is 6 kΩ and input resistance 1 kΩ, calculate its voltage gain.
(ii) Why is a semiconductor damaged by strong current? *(Delhi 2008)*

SA II (3 marks)

77. (i) Write the functions of three segments of a transistor.
(ii) Draw the circuit diagram for studying the input and output characteristics of *n-p-n* transistor in common emitter configuration. Using the circuit, explain how input, output characteristics are obtained. *(Delhi 2016)*

78. For a CE-transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100, find the input signal voltage

and base current, if the base resistance is 1 kΩ. *(AI 2016)*

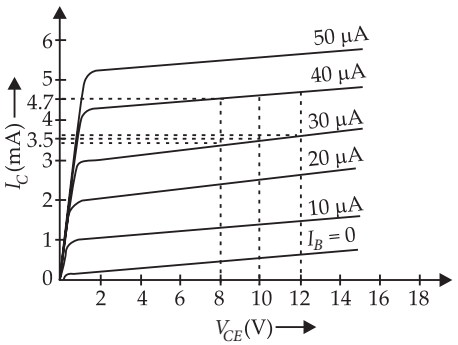
79. Draw a circuit diagram of a transistor amplifier in CE configuration.
Define the terms : (i) Input resistance and (ii) Current amplification factor. How are these determined using typical input and output characteristics? *(Delhi 2015)*

80. Draw a circuit diagram of a CE transistor amplifier. Briefly explain its working and write the expression for (i) current gain, (ii) voltage gain of the amplifier. *(AI 2015)*

81. (a) Draw a plot of transfer characteristic (V_0 vs V_i) and show which portion of the characteristic is used in amplification and why?
(b) Draw the circuit diagram of base bias transistor amplifier in CE configuration and briefly explain its working. *(AI 2015C)*

82. Draw a circuit diagram of *n-p-n* transistor amplifier in CE configuration. Under what condition does the transistor act as an amplifier? *(AI 2014)*

83. Output characteristics of an *n-p-n* transistor in CE configuration is shown in the figure. Determine:
(i) Dynamic output resistance
(ii) d.c. current gain and
(iii) a.c. current gain at an operating point V_{CE} = 10 V, when I_B = 30 μA. *(Delhi 2013)*



84. Draw the transfer characteristic of a base-biased transistor in CE configuration. Mark the regions where the transistor can be used as switch. Explain briefly its working. *(Delhi 2012C)*

85. Draw transfer characteristics of common emitter *n-p-n* transistor. Point out the region in which the transistor operates as an amplifier. Define the following terms used in transistor amplifiers:
(i) Input resistance
(ii) Output resistance
(iii) Current amplification factor. *(Foreign 2011)*

86. (i) Draw the general shape of the 'transfer characteristics' of a transistor in its CE configuration.
Which regions of this characteristic of a transistor, are used when it work (a) as a switch, (b) as an amplifier?
(ii) Why is the output voltage of the CE amplifier opposite in phase with the input voltage? *(AI 2010C)*

87. Draw the labelled circuit diagram of a common -emitter transistor amplifier. Explain clearly how the input and output signals are in opposite phase. *(AI 2008)*

88. State briefly the underlying principle of a transistor oscillator. Draw a circuit diagram, show how the feedback is accomplished by inductive coupling. Explain the oscillator action. *(AI 2008)*

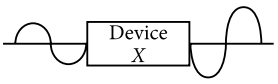
89. Draw the circuit diagram of a common emitter amplifier using *n-p-n* transistor. What is the phase difference between the input signal and output voltage? State two reasons why a common emitter amplifier is preferred over a common base amplifier. *(AI 2007)*

VBQ (3 marks)

90. Gautam went for a vacation to the village where his grandmother lived. His grandmother took him to watch 'nautanki' one evening. They noticed a blackbox connected to the mike lying nearby. Gautam's grandmother did not know what that box was. When she asked this question to Gautam, he explained to her that it was an amplifier.
(i) Which values were displayed by the grandmother? How can inculcation of these values in students be promoted?
(ii) What is the function of an amplifier?
(iii) Which basic electronic device is used in the amplifer? *(Foreign 2016)*

LA (5 marks)

91. (a) Figure shows the input waveform which is converted by a device '*X*' into an output waveform. Name the device and explain its working using the proper circuit. Derive the expression for its voltage gain and power gain.



(b) Draw the transfer characteristic of base biased transistor in CE configuration. Explain clearly which region of the curve is used in an amplifier. *(Delhi 2015C)*

92. (a) Differentiate between segments of a transistor on the basis of their size and level of doping.

(b) How is transistor biased to be in active state?

(c) With the help of necessary circuit diagram, describe briefly how *n-p-n* transistor in *CE* configuration amplifies a small sinusoidal input voltage. Write the expression for the a.c. current gain. *(Delhi 2014)*

93. Describe briefly the underlying principle of a transistor amplifier working as an oscillator. Hence, use the necessary circuit diagram to explain how self sustained oscillations are achieved in the oscillator. *(3/5, Delhi 2014C)*

94. (a) Draw the circuit diagram of an *n-p-n* transistor with emitter-base junction forward biased and collector-base junction reverse biased. Describe briefly how the motion of charge carriers in the transistor constitutes the emitter current (I_E), the base current (I_B) and the collector current (I_C). Hence deduce the relation $I_E = I_B + I_C$.

(b) Explain with the help of circuit diagram how a transistor works as an amplifier.

(AI 2014C)

95. Draw the circuit arrangement for studying the input and output characteristics of *n-p-n* transistor in CE configuration.

Draw the typical nature of these input and output characteristics. Explain how these are obtained.

Define the terms (i) input resistance and (ii) current amplification factor. *(Foreign 2013)*

96. (a) Why is the base region of a transistor thin and lightly doped?

(b) Draw the circuit diagram for studying the characteristics of an *n-p-n* transistor in common emitter configuration.

Sketch the typical (i) input and (ii) output characteristics can be used to obtain the current gain of the transistor. *(Delhi 2013C)*

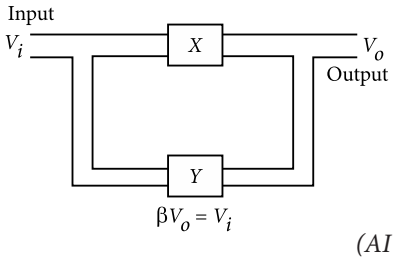
97. Draw a simple circuit of a *CE* transistor amplifier. Explain its working. Show that the voltage gain, A_V, of the amplifier is given by $A_V = -\frac{\beta_{ac} R_L}{r_i}$, where β_{ac} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain? *(Delhi 2012)*

98. (a) Draw the circuit for studying the input and output characteristics of an *n-p-n* transistor in CE configuration. Show, how from the output characteristics, the information about the current amplification factor (β_{ac}) can be obtained.

(b) Draw a plot of the transfer characteristic (V_0) versus (V_i) for a base-biased transistor in CE configuration. Show for which regions in the plot, the transistor can operate as a switch.

(Foreign 2012)

99. The set-up shown below can produce an a.c. output without any external input signal. Identify the components '*X*' and '*Y*' of this set-up. Draw the circuit diagram for this set-up. Describe briefly its working.



(AI 2012C)

100. Using the necessary circuit diagram, draw the transfer characteristics of a base-biased transistor in CE, configuration. With the help of these characteristics explain briefly how the transistor can be used as an amplifier.

(3/5, Delhi 2011C)

101. With the help of the circuit diagram explain the working principle of a transistor amplifier as an oscillator. *(3/5, Delhi 2010)*

102. (a) Draw the circuit arrangement for studying the input and output characteristics of an *n-p-n* transistor in CE configuration. With the help of these characteristics define (i) input resistance,
(ii) current amplification factor.
(b) Describe briefly with the help of a circuit diagram how an *n-p-n* transistor is used to produce self-sustained oscillations.
(AI 2010)

103. Draw the circuit diagram of a base-biased *n-p-n* transistor in CE configuration. Explain how this circuit is used to obtain the transfer characteristic (V_o – V_i characteristics). How do we explain the working of a transistor as a switch using the characteristic?
(Foreign 2010)

104. (a) Draw the circuit diagram used for studying the input and output characteristics, of an *n-p-n* transistor, in its CE configuration. Show the typical shapes of these two characteristics.
(b) How are the (i) input resistance and (ii) current amplification factor of the transistor determined from these characteristics?
(Delhi 2010C)

105. (i) Draw a circuit diagram to study the input and output characteristics of an *n-p-n* transistor in its common emitter configuration. Draw the typical input and output characteristics.
(ii) Explain, with the help of a circuit diagram, the working of *n-p-n* transistor as a common emitter amplifier.
(Delhi 2009)

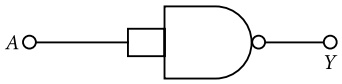
106. Draw the symbolic representation of a (i) *p-n-p*, (ii) *n-p-n* transistor. Why is the base region of transistor thin and lightly doped? With proper circuit diagram, show the biasing of a *p-n-p* transistor in common base configuration. Explain the movement of charge through different parts of the transistor in such a configuration and show that $I_E = I_C + I_B$.
(Delhi 2007)

14.10 Digital electronics and logic gates

VSA (1 mark)

107. Draw the logical symbol of NAND gate and give its truth table. *(AI 2015C)*

108. Write the truth table for a NAND gate as shown in the figure.



(AI 2013C)

109. Draw the logic circuit of NAND gate and write its truth table. *(Foreign 2011)*

110. A given logic gate inverts the input applied to it. Name this gate and give its symbol.
(Delhi 2010C)

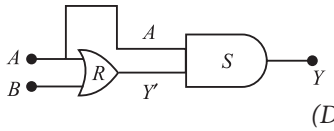
111. The truth table, of a logic gate, has the form given here. Name this gate and draw its symbol.

A	*B*	*Y*
0	0	1
0	1	0
1	0	0
1	1	0

(AI 2010C)

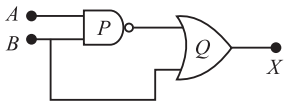
SA I (2 marks)

112. Write the truth table for the combination of the gates shown. Name the gates used.



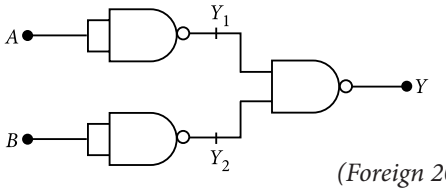
(Delhi 2014)

113. Identify the logic gates marked '*P*' and '*Q*' in the given circuit. Write the truth table for the combination.



(Delhi 2014)

114. Identify the equivalent gate represented by the circuit shown in the figure. Draw its logic symbol and write the truth table.

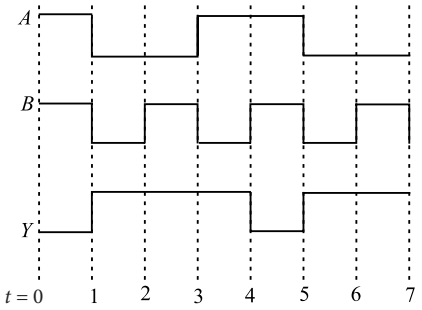


(Foreign 2014)

115. The outputs of two NOT gates are fed to a NOR gate. Draw the logic circuit of the combination of gates. Give its truth table. Identify the gate represented by this combination.

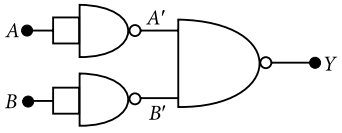
(Delhi 2014C)

116. The input waveforms '*A*' and '*B*' and output waveform '*Y*' of a gate are shown below. Name the gate it represents, write its truth table and draw the logic symbol of this gate.



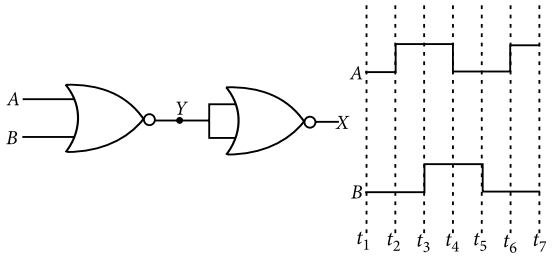
(AI 2014C, AI 2009)

117. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



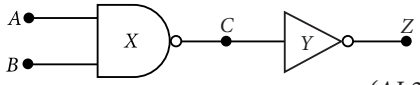
(AI 2013)

118. Draw the output waveform at *X*, using the given inputs *A* and *B* for the logic circuit shown below. Also, identify the logic operation performed by this circuit.



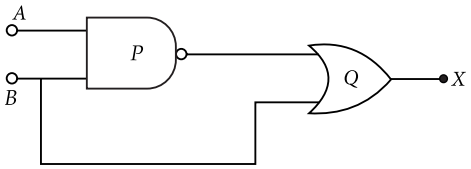
(Delhi 2011)

119. Identify the logic gates '*X*' and '*Y*' in the figure. Write down the truth table for output *Z* for all possible inputs '*A*' and '*B*'.



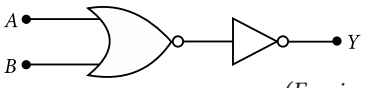
(AI 2011C)

120. (i) Identify the logic gates marked *P* and *Q* in the given logic circuit.



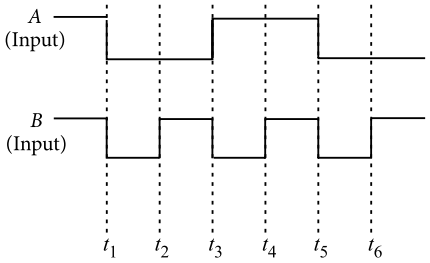
(ii) Write down the output at *X* for the inputs $A = 0, B = 0$ and $A = 1, B = 1$. *(AI 2010)*

121. Write the truth table for the following circuit. Name the equivalent gate that this circuit represents.



(Foreign 2010)

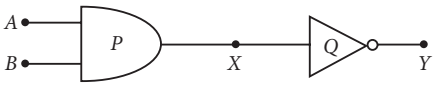
122. The given inputs *A*, *B* are fed to 2-input NAND gate. Draw the output wave form of the gate.



(Delhi 2008)

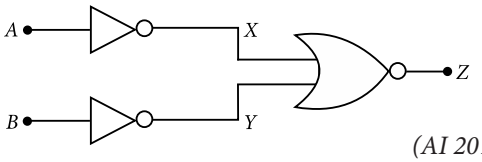
SA II (3 marks)

123. Identify the gates *P* and *Q* shown in the figure. Write the truth table for the combination of the gates shown.



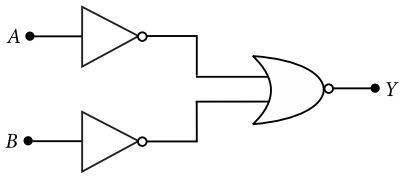
Name the equivalent gate representing this circuit and draw its logic symbol. *(AI 2015)*

124. You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate corresponds to it.



(AI 2011)

125. The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below.



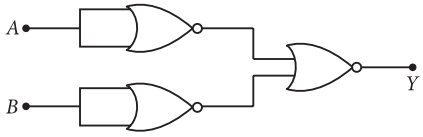
Analyse the action of the gates (1) and (2) and indentify the logic gate of the complete circuit so obtained. Give its symbol and the truth table.

(AI 2008)

LA (5 marks)

126. Identify the logic gate equivalent to the circuit shown in the figure.

Draw the truth table for all possible values of inputs A and B.

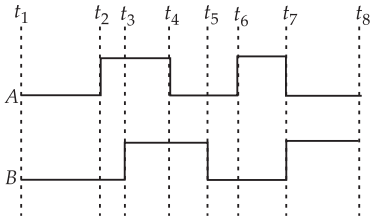


(2/5, Delhi 2015C)

127. Show the output waveforms (Y) for the following inputs A and B of

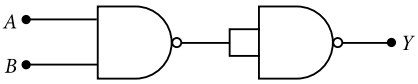
(i) OR gate

(ii) NAND gate.



(2/5, AI 2014C)

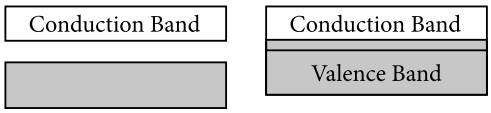
128. Identify the logic gate represented by the circuit as shown and write its truth table.



(2/5, Delhi 2010)

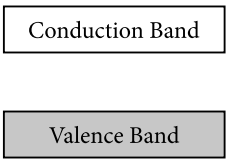
Detailed Solutions

1. Metals : (i) For metals, the valence band is completely filled and the conduction band can have two possiblities-either it is partially filled with an extremely small energy gap between the valence and conduction bands or it is empty, with the two bands overlapping each other as shown below



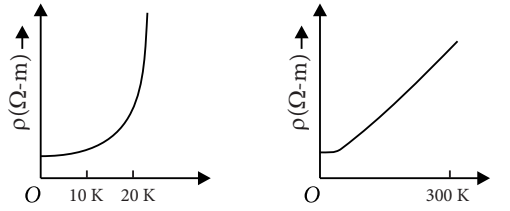
(ii) On applying even an small electric field, metals can conduct electricity.

Insulators : (i) for insulator, the energy gap between the conduction and valence bands is very large. Also, the conduction band is practically empty, as shown below

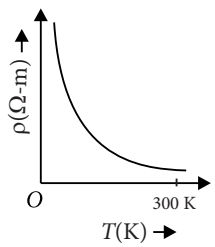


(ii) When an electric field is applied across such a solid, the electrons find it difficult to acquire such a large amount of energy to reach the conduction band. Thus, the conduction band continues to be empty. That is why no current flows through insulators.

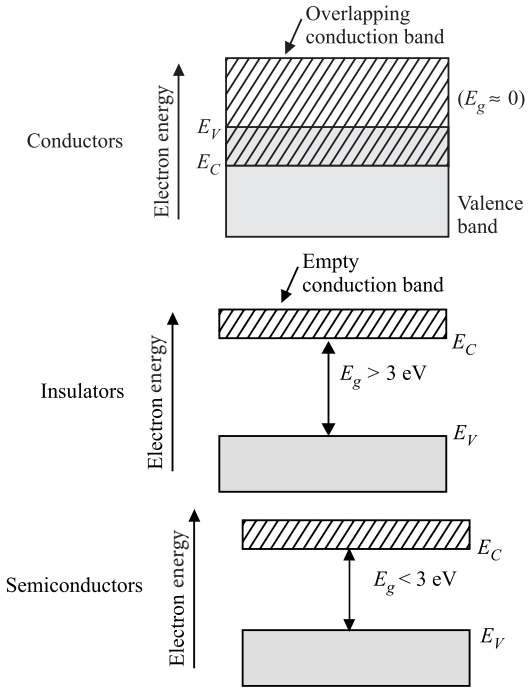
2. (i) The resistivity of a conductor increases non-linearly with increase in temperature.



(ii) The resistivity of a semiconductor decreases with increase in temperature.



3.



Two Distinguishing features :

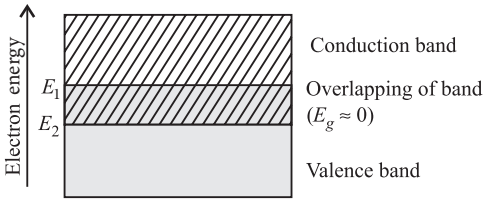
(i) In conductors, the valence band and conduction band tend to overlap (or nearly overlap) while in insulators they are separated by a large energy gap and in semiconductors are separated by a small energy gap.

(ii) The conduction band of a conductor has a large number of electrons available for electrical conduction. However, the conduction band of insulators is almost empty while that of the semiconductor has only a (very) small number of such electrons available for electrical conduction.

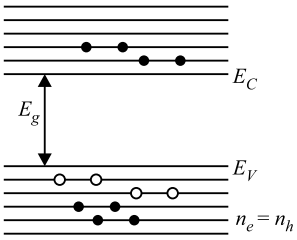
4. When two atoms come closer to each other their valence electrons begin to interact with each other. Due to this interaction energy levels of valence electrons get modified. This process is called splitting of energy levels. Splitting of energy levels in case of a crystal results in the formation of energy bands. Completely filled energy levels form valence band and vacant energy levels form conduction band. The energy bands are separated by an energy gap (E_g) called energy band gap..

Energy band diagrams (at $T > 0$ K),

(i) For a conductor :



(ii) For an intrinsic semiconductor :



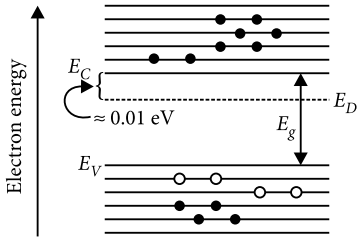
5.

	***n*-type Semiconductor**	***p*-type Semiconductor**
(i)	It is formed by doping pentavalent impurities.	It is formed by doping trivalent impurities.
(ii)	The electrons are majority carriers and holes are minority carriers. ($n_e >> n_h$)	The holes are majority carriers and electrons are minority carriers. ($n_h >> n_e$)

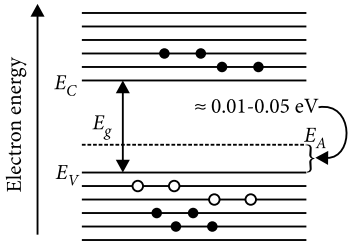
6.

	Intrinsic Semiconductors	**Extrinsic Semiconductors**
1.	These are pure semiconducting tetravalent crystals.	These are semi-conducting tetravalent crystals doped with impurity atoms of group III or V.
2.	Their electrical conductivity is low.	Their electrical conductivity is high.
3.	There is no permitted energy state between valence and conduction bands.	There is permitted energy state of the impurity atom between valence and conduction bands.

7. The required energy band diagrams are given below:



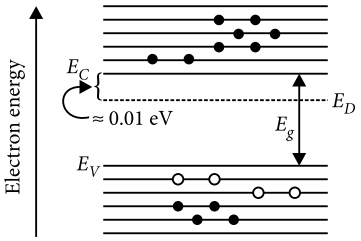
(a)
Energy band diagram of *n*-type semiconductor at $T > 0$ K



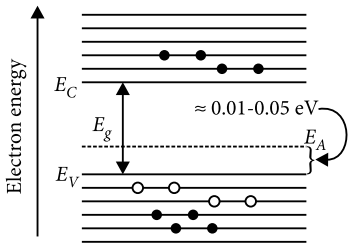
(b)
Energy band diagram of *p*-type semiconductor at $T > 0$ K

8. *Refer to answer 5.*

9. (i)



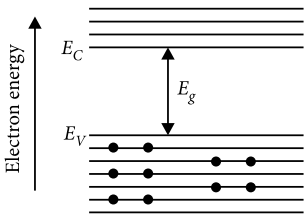
(a)
Energy band diagram of *n*-type semiconductor at $T > 0$ K



(b)
Energy band diagram of *p*-type semiconductor at $T > 0$ K

In *n*-type extrinsic semiconductors, the number of free electrons in conduction band is much more than the number of holes in valence band. The donor energy level lies just below the conduction band. In *p*-type extrinsic semiconductor, the number of holes in valence band is much more than the number of free electrons in conduction band. The acceptor energy level lies just above the valence band.

(ii)



Energy band diagram of semiconductor at $T = 0$ K

At absolute zero temperature (0 K) conduction band of semiconductor is completely empty, *i.e.,* $\sigma = 0$. Hence the semiconductor behaves as an insulator. At room temperature, some valence electrons acquire enough thermal energy and jump to the conduction band where they are free to conduct electricity. Thus the semiconductor acquires a small conductivity at room temperature.

10. *Refer to answer 7.*

The donor energy level E_D is just below the bottom of the conduction band. At room temperature this small energy gap is easily converted by the thermally excited electrons. The conduction band has more electrons as they have been contributed both by thermal excitation and donor impurities. Whereas the acceptor energy level E_A lies slightly above the top of the valence band. At room temperature, many electrons of the valence band get excited to these acceptor energy levels, leaving behind equal number of holes in the valence band. These holes can conduct current. Thus the valence band has more holes than the electrons in the conduction band.

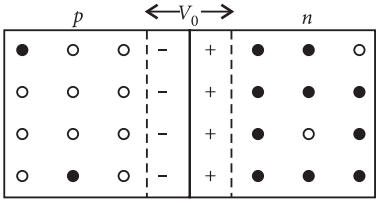
11.

	Intrinsic semiconductor	***P*-type semiconductor**
1.	It is a semiconductor in pure form.	It is a semiconductor doped with trivalent (like Al, In) impurity.
2.	Intrinsic charge carriers are electrons and holes with equal concentration.	Majority charge carriers are holes and minority charge carriers are electrons.
3.	Conductivity depends on temperature.	Conductivity depends on temperature as well as dopant concentration.

In *p*-type semiconductor, trivalent impurity is doped with tetravalent pure semiconductor. Both type of atom (impurity and host semiconductor) are electrically neutral and hence, so produced *p*-type semiconductor is electrically neutral.

12. Any slab, howsoever flat, will have roughness much larger than the inter-atomic crystal spacing (~2 to 3Å) and hence continuous contact at the atomic level will not be possible. The junction will behave as a discontinuity for the flowing charge carriers.

13.



When *p*-*n* junction is formed, diffusion of charge take place at the junction where free electrons from *n*-type diffuse over to *p*-type, thereby recombining with holes in *p*-type. Due to this a layer of positive charge is built on *n*-side and a layer of negative charge is built on *p*-side of the *p*-*n* junction. This sets up potential difference across the junction and an internal electric field E_i directed from *n*-side to *p*-side. Due to this field, an electron on *p*-side of the junction moves to *n*-side and a hole on *n*-side moves to *p*-side. This motion of charge carriers due to electric field is called drift. E_i becomes strong enough so that the layer sufficiently grows up within a very short time of the junction being formed, preventing any further movement of charge carriers (*i.e.* electrons and holes) across the junction. Thus a potential difference V_0 of the order of 0.1 to 0.3 V is set up across the *p*-*n* junction called potential barrier or junction barrier potential. The thin region on either side of the junction is formed containing

immobile positive and negative charges is known as depletion layer.

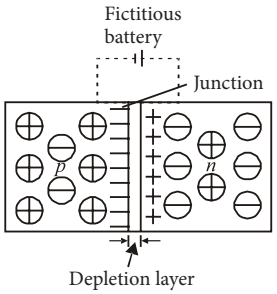
14. *Refer to answer 13.*

15. *Refer to answer 13.*

16. *Refer to answer 13.*

17. *Refer to answer 13.*

18.



The two processes are

(i) Diffusion (ii) Drift

Diffusion : Holes diffuse from p-side to n-side ($p \rightarrow n$) and electrons diffuse from n-side to p-side($n \rightarrow p$)

Drift : The motion of charge carriers, due to the applied electric field ($\vec{E}$) which results in drifting of holes along $\vec{E}$ and of electrons opposite to that of electric field.

19. *Refer to answer 13.*

20. (i) Forward biased : As forward voltage opposes the potential barrier and effective barrier potential decreases. It makes the width of the depletion layer smaller.

(ii) Reverse biased : As reverse voltage supports the potential barrier and effective barrier potential increases. It makes the width of the depletion layer larger.

21. (i) From the given curve, we have

voltage, $V = 0.8$ volt for current, $I = 20$ mA

voltage, $V = 0.7$ volt for current, $I = 10$ mA

$\Rightarrow \quad \Delta I = (20 - 10)\text{mA} = 10 \times 10^{-3}$ A

$\Rightarrow \quad \Delta V = (0.8 - 0.7) = 0.1$ V

$\therefore$ Resistance, $R = \dfrac{\Delta V}{\Delta I}$

$\Rightarrow \quad R = \dfrac{0.1}{10 \times 10^{-3}} \Rightarrow R = 10\ \Omega$

(ii) For $V = -10$ V, we have

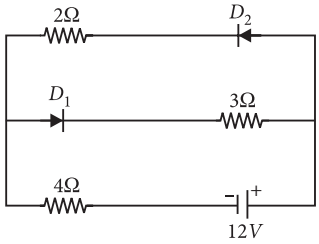
$I = -1\ \mu\text{A} = -1 \times 10^{-6}$ A

$\Rightarrow \quad R = \dfrac{10}{1 \times 10^{-6}} = 1.0 \times 10^{7}\ \Omega$

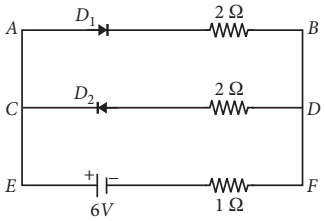
22. (i) Diode D_1 is reverse biased, so it offers an infinite resistance. So no current flows in the branch of diode D_1.

(ii) Diode D_2 is forward biased, and offers negligible resistance in the circuit. So current in the branch

$$I = \frac{V}{R_{eq}} = \frac{12V}{2\Omega + 4\Omega} = 2A$$



23. According to the question

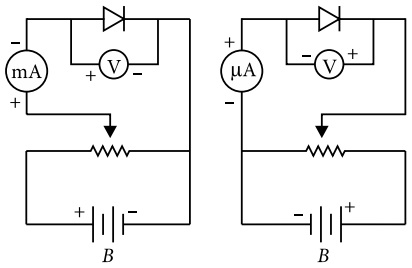


$R_{AB} = 2 + 1 = 3\ \Omega$

$$\frac{1}{R'} = \frac{1}{2} + \frac{1}{3} = \frac{3+2}{6} = \frac{5}{6}\ \Omega^{-1}; R' = \frac{6}{5}\ \Omega$$

$$I_{EF} = \frac{V}{R'} = \frac{6}{6/5} = 5\ \text{A}$$

24. Circuit diagram of forward biased and reverse biased p-n junction diode is shown below :

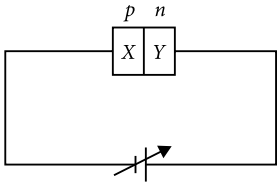


The width of depletion layer

(i) decreases in forward bias

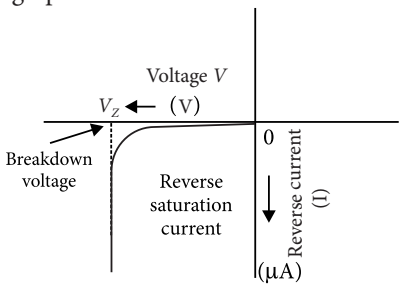
(ii) increases in reverse bias

25. Semiconductor material (germanium) X is doped with indium which is trivalent. So it forms p-type semiconductor. Similarly, the semiconductor Y is doped with arsenic which is pentavalent. So it forms n-type semiconductor.

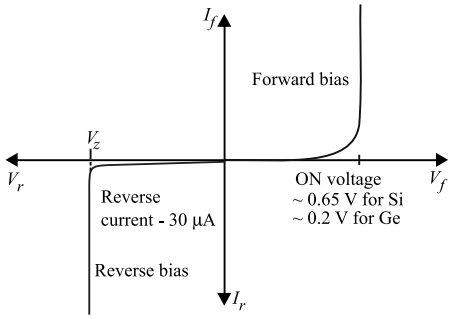


(i) Junction is reverse biased.

(ii) *V-I* graph



26.

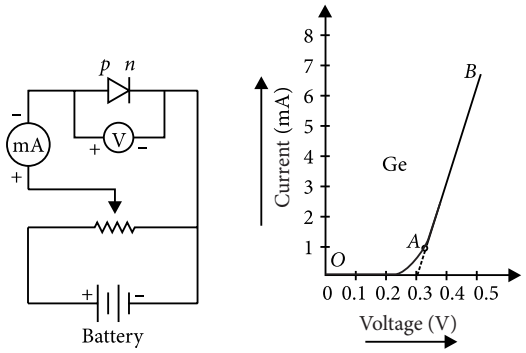


(i) The reverse current is due to minority charge carriers and even a small voltage is sufficient to sweep the minority carriers from one side of the junction to the other side of the junction. Here the current is not limited by the magnitude of the applied voltage but is limited due to the concentration of the minority carrier on either side of the junction.

(ii) At critical voltage/breakdown voltage, a large number of covalent bonds break, resulting in availability of large number of charge carriers.

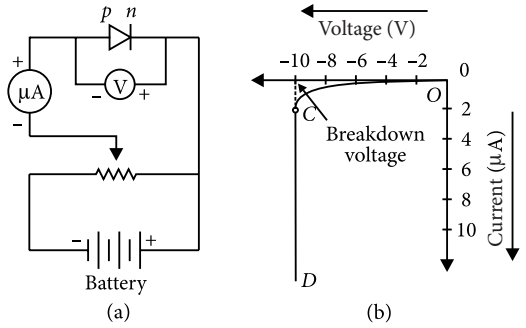
Zener diode operates under the reverse bias in the breakdown region.

27. (a) Forward biased characteristics : The circuit diagram for studying forward biased characteristics is shown in the figure. Starting from a low value, forward bias voltage is increased step by step (measured by voltmeter) and forward current is noted (by ammeter). A graph is plotted between voltage and current. The curve so obtained is the forward characteristic of the diode.



At the start when applied voltage is low, the current through the diode is almost zero. It is because of the potential barrier, which opposes the applied voltage. Till the applied voltage exceeds the potential barrier, the current increases very slowly with increase in applied voltage (*OA* portion of the graph). With further increase in applied voltage, the current increases very rapidly (*AB* portion of the graph), in this situation, the diode behaves like a conductor. The forward voltage beyond which the current through the junction starts increasing rapidly with voltage is called threshold or cut-in voltage. If line *AB* is extended back, it cuts the voltage axis at potential barrier voltage.

(b) Reverse biased characteristics : The circuit diagram for studying reverse biased characteristics is shown in the figure.



In reverse biased, the applied voltage supports the flow of minority charge carriers across the junction. So, a very small current flows across the junction due to minority charge carriers.

Motion of minority charge carriers is also supported by internal potential barrier, so all the minority carriers cross over the junction.

Therefore, the small reverse current remains almost constant over a sufficiently long range of reverse bias, increasing very little with increasing voltage (OC portion of the graph). This reverse current is voltage independent upto certain voltage known as breakdown voltage and this voltage independent current is called reverse saturation current.

28. *Refer to answer 27.*

29. If *p*-type and *n*-type semiconductor are heavily doped. Then due to diffusion of electrons from *n*-region to *p*-region, and of holes from *p*-region to *n*-region, a depletion region formed of size of order less than 1 μm. The electric field directing from *n*-region to *p*-region produces a reverse bias voltage of about 5 V and electric field becomes very large.

$$\vec{E} = \frac{\Delta V}{\Delta x} = \frac{5V}{1\,\mu m} \approx 5\times10^{6}\ \text{V/m}$$

30. Depletion layer : The small region in the vicinity of the junction which is depleted of free charge carriers and has only immobile ions is called the depletion layer.

Barrier potential : Due to accumulation of negative charges in the *p*-region and positive charges in the *n*-region sets up a potential difference across the junction sets up. This acts as a barrier and is called potential barrier V_B which opposes the further diffusion of electrons and holes across the junction.

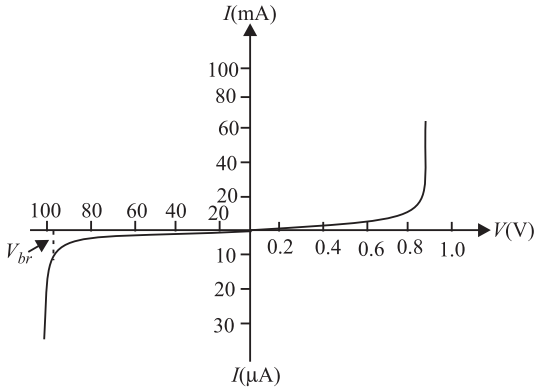
(i) An increase in doping concentration, the applied potential difference causes an electric field which acts opposite to the potential barrier. This results in reducing the potential barrier and hence the width of depletion layer decreases.

(ii) In forward biasing the width of depletion layer reduced and the external applied field is able to overcome the strong electric field of depletion layer. In reverse biasing the width of depletion layer increases and the electric field of depletion layer become more stronger.

31. *Refer to answers 13 and 30(ii).*

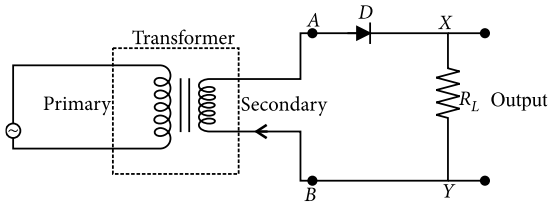
32. *Refer to answer 27.*

The battery is connected to the silicon diode through a potentiomenter, so that the applied voltage can be changed. For different value of voltage, the value of current is noted.

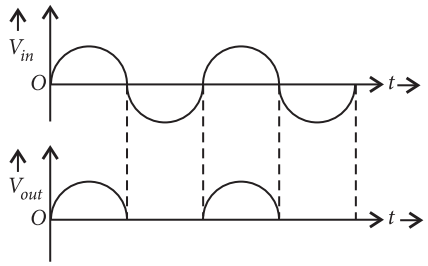


V-I Characteristics of a Silicon diode

33. Half wave rectifier:

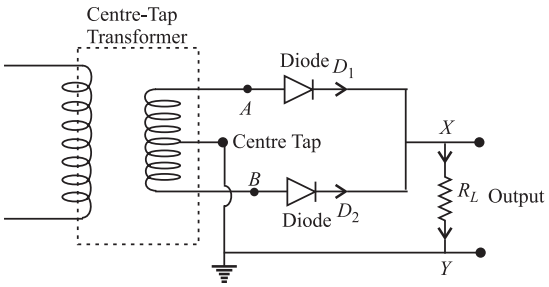


It consists of a diode *D* connected in series with load resistor R_L across the secondary windings of a step-down transformer. Primary of transformer is connected to a.c. supply. During positive half cycle of input a.c., end *A* of the secondary winding becomes positive and end *B* negative. Thus, diode *D* becomes forward biased and conducts the current through it. So, current in the circuit flows from *A* to *B* through load resistor R_L.



During negative half cycle of input a.c., end *A* of the secondary winding becomes negative and end *B* positive. Thus, diode *D* becomes reverse biased and does not conduct any current. So, no current flows in the circuit. Since electric current through load R_L flows only during positive half cycle, in one direction only *i.e.*, from *A* to *B*, so d.c. is obtained across R_L.

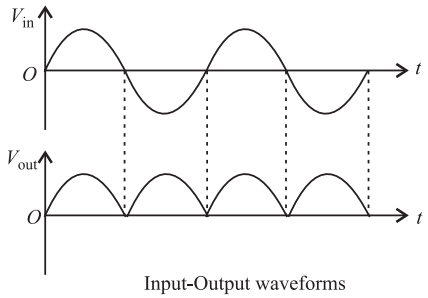
34. Full Wave Rectifier



A full wave rectifier consists of two diodes connected in parallel across the ends of secondary winding of a center tapped step down transformer. The load resistance R_L is connected across secondary winding and the diodes between A and B as shown in the circuit.

During positive half cycle of input a.c., end A of the secondary winding becomes positive and end B negative. Thus diode D_1 becomes forward biased, whereas diode D_2 reverse biased. So diode D_1 allows the current to flow through it, while diode D_2 does not, and current in the circuit flows from D_1 and through load R_L from X to Y.

During negative half cycle of input a.c., end A of the secondary winding becomes negative and end B positive, thus diode D_1 becomes reverse biased, whereas diode D_2 forward biased. So diode D_1 does not allow the current to flow through it but diode D_2 does, and current in the circuit flows from D_2 and through load R_L from X to Y.



Input-Output waveforms

Since in both the half cycles of input a.c., electric current through load R_L flows in the same direction, so d.c. is obtained across R_L. Although direction of electric current through R_L remains same, but its magnitude changes with time, so it is called pulsating d.c.

35. *Refer to answer 34.*

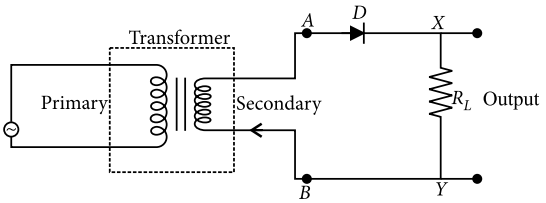
(ii) A full wave rectifier gives a continuous, unidirectional but pulsating output voltage or current. The rectified ouput is passed through a filter circuit which removes the ripple and an almost steady d.c. output (voltage or current) is obtained.

36. *Refer to answer 33.*

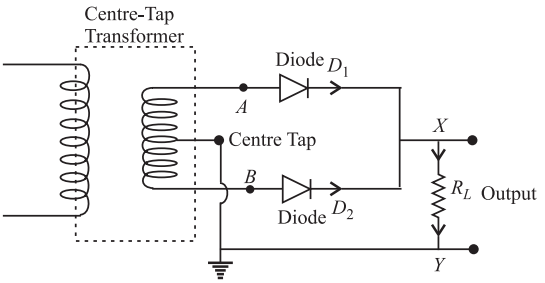
37. *Refer to answer 34.*

38. *Refer to answer 34.*

39. (a) X = Half wave rectifier
Y = Full wave rectifier



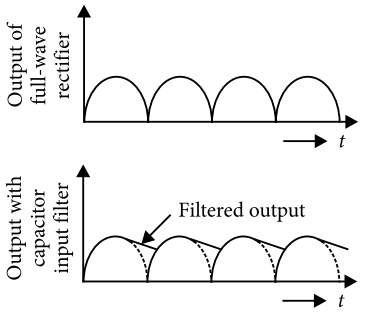
(Half wave rectifier)



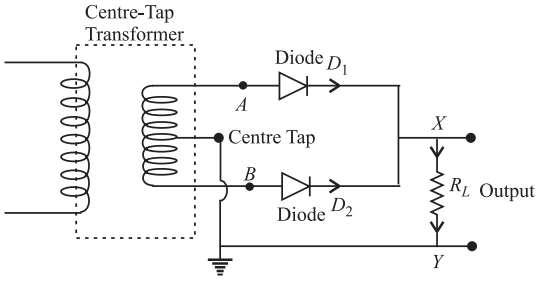
(Full wave rectifier)

(b) *Refer to answer 34.*

(c) A capacitor of large capacitance is connected in parallel to the load resistor R_L. When the pulsating voltage supplied by the rectifier is rising, the capacitor C gets charged. If there is no external load, the capacitor would have remained charged to the peak voltage of the rectified output. However, when there is no load and the rectified voltage starts falling, the capacitor gets discharged through the load and the voltage across capacitor begins to fall slowly.



40. Device '*X*' is a full wave rectifier.



41. Rectifier is a circuit which converts alternating current (a.c.) into direct current (d.c.). The principle on which rectifier works is that a *p-n* junction diode is unidirectional device, *i.e.*, it allows the current to flow through it only in one direction, when it is in forward bias.

Refer to answer 34.

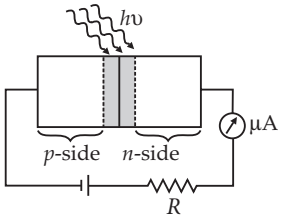
42. Region *BC* of the graph has a negative slope, hence in region *BC* semiconductor has a negative resistance.

43. Photodiode is used to detect the light signal and to measure light intensity.

44. The device is zener diode. The zener diode is used as voltage regulator.

45. In solar radiations, intensity is maximum near 1.5 eV. In GaAs (Gallium Arsenide), $E_g \approx 1.53$ eV, so solar cell made of GaAs has high absorption coefficient of solar radiations.

46. Working of photodiode : A junction diode made from light sensitive semiconductor is called a photodiode. A photodiode is a *p-n* junction diode arranged in reverse biasing.



The number of charge carriers increases when light of suitable frequency is made to fall on the *p-n* junction, because new electron holes pairs are created by absorbing the photons of suitable frequency. Intensity of light controls the number of charge carriers. Due to this property photodiodes are used to detect optical signals.

47. (a) (i) There is very little resistance to limit the current in LED. Therefore, a resistor must be used in series with the LED to avoid any damage to it.

(ii) The reverse breakdown voltages of LEDs are very low, typically around 5 V. So care should be taken while fabricating a *p-n*-junction diode so that the *p* side should only attached to the positive of battery and vice versa as LED easily get damaged by a small reverse voltages.

(b) The semiconductor used for fabrication of visible LEDs must have at least a band gap of 1.8 eV because spectral range of visible light is about 0.4 μm to 0.7 μm, *i.e.*, about 3 eV to 1.8 eV.

48. Consider the case of an *n*-type semiconductor. The majority carrier density (n) is considerably larger than the minority hole density p (*i.e.*, $n >> p$). On illumination, let the excess electrons and holes generated be Δn and Δp, respectively :

$$n' = n + \Delta n$$
$$p' = p + \Delta p$$

Here n' and p' are the electron and hole concentrations at any particular illumination and n and p are carriers concentration when there is no illumination. Remember $\Delta n = \Delta p$ and $n > > p$. Hence, the fractional change in the majority carriers (*i.e.*, $\Delta n/n$) would be much less than that in the minority carriers (*i.e.*, $\Delta p/p$). In general, we can state that the fractional change due to the photo-effects on the minority carrier dominated reverse bias current is more easily measurable than the fractional change in the forward bias current. Hence, photodiodes are preferably used in the reverse bias condition for measuring light intensity.

49. A light emitting diode is simply a forward biased *p-n* junction which emits spontaneous light radiation. At the junction, energy is released in the form of photons due to the recombination of the excess minority charge carrier with the majority charge carrier.

Advantages :

(i) Low operational voltage and less power.

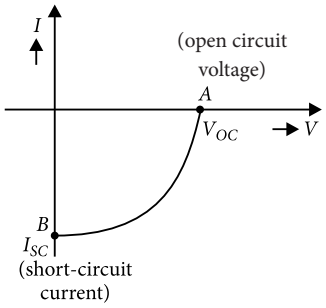
(ii) Fast action and no warm up time required.

50. (a) The energy for the maximum intensity of the solar radiation is nearly 1.5 eV. In order to have photo excitation the energy of radiation ($h\nu$) must be greater than energy band gap (E_g), *i.e.*, $h\nu > E_g$. Therefore, the semiconductor with energy band gap

about 1.5 eV or lower and with higher absorption coefficient, is likely to give better solar conversion efficiency.

The energy band gap for Si is about 1.1 eV, while for GaAs, it is about 1.53 eV. The gas GaAs is better inspite of its higherband gap than Si because it absorbs relatively more energy from the incident solar radiations being of relatively higher absorption coefficient.

(b)

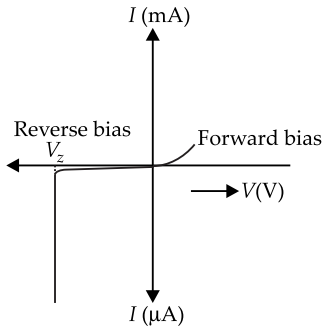


(i) *V-I* curve is drawn in the forth quadrant, because a solar cell deos not draws current but supply current to the load.

(ii) In *V-I* curve, the point *A* indicates the maximum voltage V_{OC} being supplied by the given solar cell when no current is being drawn from it. V_{OC} is called the open circuit voltage.

(iii) In *V-I* curve, the point B indicates the maximum current I_{SC} which can be obtained by short circuiting the solar cell without any load resistance. I_{SC} is called the short circuit current.

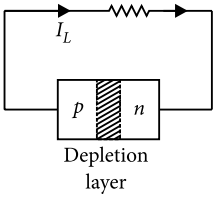
51. Zener diode



Working : The *V-I* characteristics of a Zener diode is shown in the above figure. When the applied reverse bias voltage (V) reaches the breakdown voltage (V_z) of the Zener diode, there is a large change in the current. After the breakdown voltage V_z, a large change in the current can be produced by almost insignificant change in the reverse bias voltage. In o er voltage remains constant, even though current through the Zener diode varies over a wide range. This property of the Zener diode is used for regulating supply voltages so that they are constant.

52. *Refer to answer 46.*

53. (i) Principle : A solar cell works on the principle of photo voltaic effect according to which when light photons of energy greater than energy band gap of a semiconductor are incident on *p-n* junction of that semiconductor, electron-hole pairs are generated which give rise to an emf. Thus, working principle of a solar cell is same as that of a photodiode. However, no bias is applied in a solar cell and the junction area is kept much larger so that more solar radiation may be incident.



Generation of emf : Three basic processes are involved in the generation of emf by a solar cell when solar radiations are incident on it. These are:

(a) The generation of electron-hole pairs close to the junction due to incidence of light with photo energy $h\nu \geq E_b$.

(b) The separation of electrons and holes due to the electric field of the depletion region. So, electrons are swept to *n*-side and holes to *p*-side.

(c) The electrons reaching the *n*-side are collected by the front contact and holes reaching *p*-side are collected by the back contact. Thus, *p*-side becomes positive and *n*-side become negative giving rise to a photovoltage.

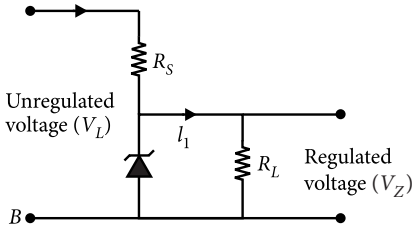
When an external load R_L is connected as shown in figure, a photocurrent I_L begins to flow through the load.

(ii) *Refer to answer 50 (a).*

54. *Refer to answers 46 and 48.*

55. (a) A zener diode is fabricated by heavily doping both *p*- and *n*-sides of the junction so that its depletion region formed is very thin and the electric field of the junction is extremely high, even for a small reverse bias voltage.

(b) Zener diode as a voltage regulator

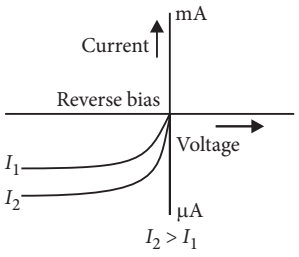


To get a constant d.c. voltage form the d.c. unregulated output of a rectifier, we use a Zener diode. The unregulated d.c. voltage is connected to the Zener diode through a series resistance R_s such that the Zener diode is reverse biased. If the input voltage increase, the current through R_s and Zener diode also increases. This increases the voltage drop across R_s without any change in the voltage across the Zener diode. Similarly, if the input voltage decreases, the current through R_s and Zener diode also decreases. The voltage drop across R_s decreases without any change in the voltage across the Zener diode. Thus any increase/decrease in the input voltage results in, increase/decrease of the voltage drop across R_s without any change in voltage across the Zener diode. Thus the Zener diode acts as a voltage regulator.

56. (a) A photodiode is fabricated by allowing light to fall on a diode through a transparent window. It is fabricated such that the generation of *e-h* pairs take place near the depletion region.

(b) *Refer to answer 46.*

V-I characteristics :

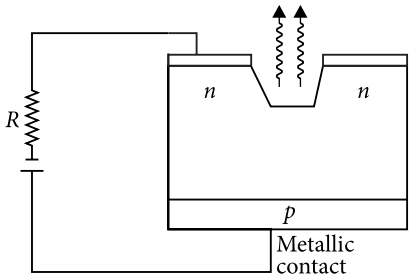


57. (i) Semiconductor diode is zener diode.
(ii) *Refer to answer 55 (b).*

58. *Refer to answer 57.*

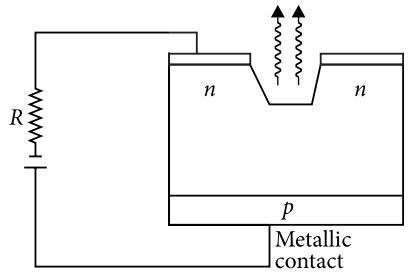
59. *Refer to answer 53.*

60. LED (Light Emitting Diode) is a forward biased *p-n* junction diode which emit spontaneous radiations.

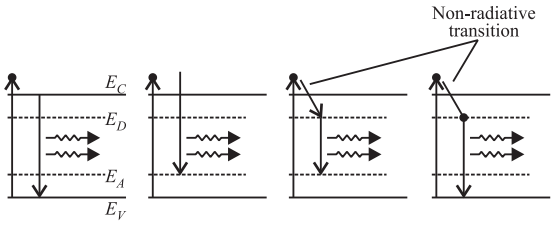


Advantages :
(i) Low operational voltage and less power.
(ii) Fast action and no warm up time required.
(iii) Long life.

61. Principle : Radiation is emitted whenever an excited electron falls from higher energy state to a lower energy state.



Working : Light emitting diode is a forward-biased *p-n* junction. Electrons are excited to higher energy state. Possible spontaneous emissions are as shown.



When electron falls from the higher to lower energy level, the energy is released in the form of light radiations. The energy of radiation emitted by LED is equal to or less than the band gap of the semiconductor.

Semiconductor used in LED is chosen according to the required wavelength of emitted radiation. To get visible wavelength least band gap required is 1.8 eV.

Advantages :
1. Low operational voltage and less power
2. Fast action and no warm up time required.

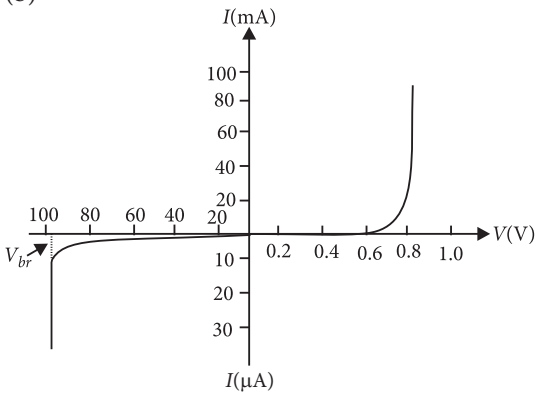
62. (i) Values displayed by Meeta, are curiosity to learn and good observation.

Values displayed by her father are patience and knowledgeable.

(ii) Meeta's father most probably explained her the benefits of using tiny bulbs (LEDs) over a single bulb.
(a) Tiny lights are semiconductor devices which consume very less power than a single bulb.
(b) Tiny lights are very cheap.
(c) If some of these tiny lights are not working, then traffic system will not be affected. But if a single bulb is fused, traffic system will be disturbed.
(iii) Tiny lights in traffic signals are called LEDs. LEDs are operated in forward biasing and emits spontaneous radiation.

63. (i) Being an engineer, Rohit was well awared about energy saving and use of modern technology.
(ii) CFLs and LEDs consumes less power in comparison of traditional incandescent lamp and also give more light and it can save upto 85% on energy bill.
(iii) The earth wire acts as negative terminal. The flowing current from positive cable to earth grounding will not be counted by electric meter because it does not pass the negative cable. In this way, you can reduce the electricity bill and save your money.

64. (a) A zener diode is considered as a special purpose semiconductor diode because it is designed to operate under reverse bias at the breakdown.
V-I characteristics of Zener diode :
(b)



We know that reverse current is due to the flow of electrons (minority carriers) from $p \rightarrow n$ and holes from $n \rightarrow p$. As the reverse bias voltage is increased, the electric field at the junction becomes significant. When the reverse bias voltage $V = V_z$. Then the electric field strength is high enough to pull valence electrons form the host atoms on the *p*-side which are accelerated to *n*-side. These electrons account for high current observed at the break down.

(c) *Refer to answer 55(b).*

65. *Refer to answer 55(b).*

66. *Refer to answer 60.*

67. *Refer to answer 55(b) and 48.*

68. Applications of LED :
(i) LEDs are used as indicator in radio and other electronic systems.
(ii) LEDs are used as optical fibre transmitters and in digital electronic circuits to show whether input are 'high' or 'low'.
Refer to answer 47(b).

69. (i) Collector current will decrease, as more of the majority carriers going from emitter to collector get neutralised in base by electron-hole combination.
(ii) Base current will increase.

70. If the value of resistor *R* is reduced, then the voltage will increase and lamp will glow more brightly.

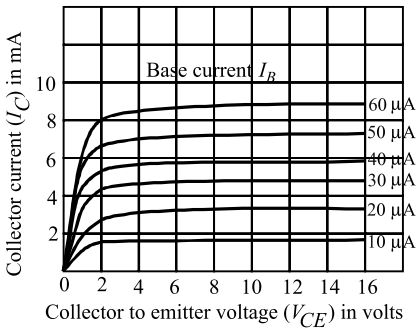
71. (i) Brightness of lamp will increase.
(ii) Voltmeter reading increases.

The given circuit is a common emitter (CE) configuration of an *n-p-n* transistor. The input circuit is forward biased and collector circuit is reverse biased.
On decreasing the resistance *R* in emitter base circuit *i.e.* input circuit the forward biasing increases, which in turn increases the emitter current , base current and collector currents.

$$I_E = I_B + I_C$$

Now due to extra collector current through lamp, the lamp will glow brighter and potential drop across it *i.e.* V also increases.

72.

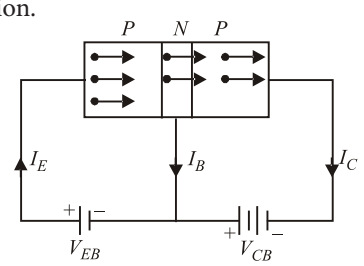


Output resistance is the reciprocal of the slope of the linear part of the output characteristics.

$$r_O = \left(\frac{\Delta V_{CE}}{\Delta I_C} \right)_{I_B}$$

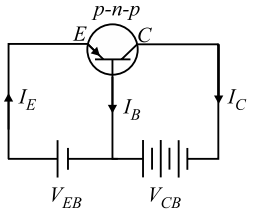
73. Action of *p-n-p* transistor :

The forward bias of the emitter-base circuit repels the holes of emitter towards the base. As the base is very thin and lightly doped, most of the holes (≈95 %) entering it pass on to collector while a very few of them (≈5 %) recombine with the electrons of the base region.



As soon as a hole combines with an electron, an electron from the negative terminal of the battery V_{EB} enters the base. This sets up a small base current I_B. Holes entering the collector region see the negative terminal of the battery V_{CB} and hence they easily reaches the collector terminal. This creates collector current I_C. Both the base current I_B and collector current I_C combine to form emitter current I_E.

$\therefore \quad I_E = I_B + I_C$



74. The transfer characteristic curve of a base biased transistor in CE configuration is shown below.

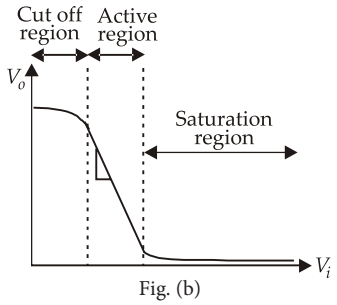


Fig. (b)

For using the transistor as an amplifier we will use the active region of the V_o versus V_i curve. The slope of the linear part of the curve represents the rate of change of the output with the input. If we consider ΔV_o and ΔV_i as small changes in the output and input voltages then $\Delta V_o/\Delta V_i$ is called the small signal voltage gain A_V of the amplifier.

75. (i) The input resistance r_i of transistor in CE configuration is defined as the ratio of small change in base emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, *i.e.*,

$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$

(ii) The current amplifiction factor of a transistor in CE configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant *i.e.*

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$

76. (i) Resistance gain $= \dfrac{R_o}{R_i} = \dfrac{6\ \text{k}\Omega}{1\ \text{k}\Omega} = 6$

Voltage gain = Current gain × Resistance gain

$= 30 \times 6 = 180$

(ii) On passing a strong current, beyond its rated value, the semiconductor diode is damaged or destroyed due to overheating.

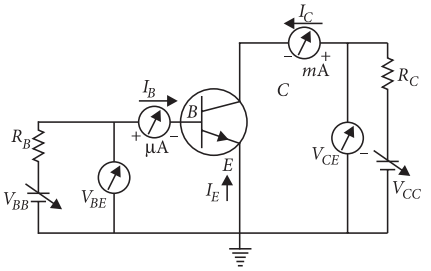
77. (i) Functions of three segments of a transistor

Emitter : It supplies a large number of majority charge carriers for the flow of current through the transistor.

Base : It controls the flow of majority charge carriers from emitter to collector.

Collector : It collects a major portion of the majority carriers supplied by emitter for the circuit operation.

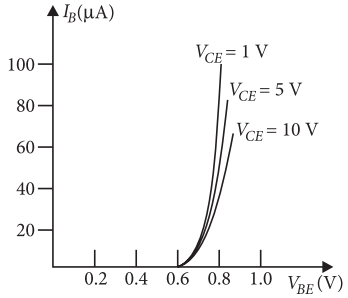
(ii)



Circuit arrangement for studying the input and output characteristics of n-p-n transistor in CE configuration.

(a) Input characteristics : Input characteristic means we have to plot the graphical representation between I_B and V_{BE}. V_{BE} is the emitter to base voltage or the forward bias voltage and I_B is the base current. In this forward biasing, *E* is at lower potential than *B*. We will be plotting I_B versus V_{BE} because base is at

higher potential than emitter, so that will be reflected here. Now go on varying V_{BE}. For silicon diode we have knee voltage around 0.7 V . After overcoming the knee voltage, current will rise sharply. The input characteristic will be different if we go on increasing the V_{CE}. It will be shifting right, means for the same V_{BE} we will be getting lower input current I_B.



Input resistance (r_i): This is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic (ac resistance) and as its value varies with the operating current in the transistor :

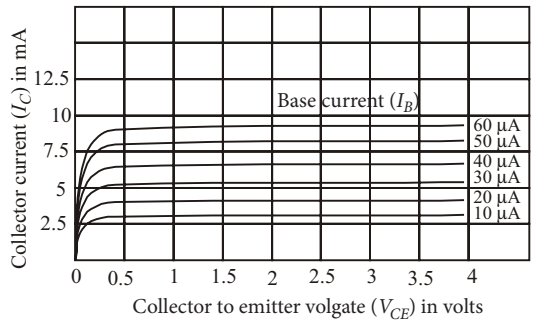
$$r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}}$$

(b) **Output characteristics :** A graph showing the variation of collector current I_C with collector-emitter voltage V_{CE} at constant base current I_B is called the output characteristic of the transistor.

A study of these curves reveals the following features:

(i) When the voltage V_{CE} increases from 0 to about 0.2 V, the collector current I_C increases rapidly.

(ii) Once the voltage V_{CE} exceeds the knee voltage the output current I_C varies very slowly but linearly with V_{CE} for a given base current I_B.



(iii) **Output resistance (r_0) :** This is defined as the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B.

$$r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$$

78. $R_C = 2\ \text{k}\Omega = 2 \times 10^3\ \Omega$, $V_{CE} = 2$ V, $\beta = 100$, $R_{in} = 1\ \text{k}\Omega = 1 \times 10^3\ \Omega$.

Collector current $I_C = \dfrac{V_{CE}}{R_C} = \dfrac{2}{2\times10^3}$

$= 1 \times 10^{-3}\text{A} = 1\ \text{mA}$

Input base current $I_B = \dfrac{I_C}{\beta} = \dfrac{1\times10^{-3}}{100}$

$= 1 \times 10^{-5}\text{A} = 10\ \mu\text{A}$

Input signal voltage,

$V_{in} = I_B \times R_{in} = 10^{-5} \times 10^3 = 10^{-2}$ V $= 10$ mV

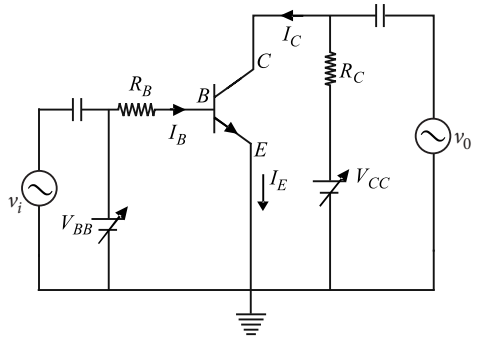
79. *Refer to answer 77 (ii).*

Current amplification factor (β) : This is defined as the ratio of the change in collector current to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is in active state.

$$\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

This is also known as small signal current gain and its value is very large.

80. To operate the transistor as an amplifier it is necessary to fix its operating point somewhere in the middle of its active region.



The working of an amplifier can be easily understood, if we first assume that $v_i = 0$. Then applying Kirchhoff's law to the output loop, we get

$V_{CC} = V_{CE} + I_C R_C$

Like wise, the input loop gives

$V_{BB} = V_{BE} + I_B R_B$

When v_i is not zero, we get

$V_{BE} + v_i = V_{BE} + I_B R_B + \Delta I_B\,(R_B + r_i)$

The change in V_{BE} can be related to the input resistance r_i and the change in I_B. Hence

$v_i = \Delta I_B (R_B + r_i) = r\Delta I_B$

The change in I_B causes a change in I_C. We define a parameter β_{ac}, which is similar to the β_{dc} defined in as

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{i_C}{i_B}$$

Which is also known as the ac current gain A_i. Usually β_{ac} is close to β_{dc} in the linear region of the output characteristics.

The change in I_C due to a change in I_B causes a change in V_{CE} and the voltage drop across the resistor R_L because V_{CC} is fixed.

These changes can be given by as

$\Delta V_{CC} = \Delta V_{CE} + R_L \Delta I_C = 0$

or $\Delta V_{CE} = -R_L \Delta I_C$

The change in V_{CE} is the output voltage v_0. From we get

$v_0 = \Delta V_{CE} = -\beta_{ac} R_L \Delta I_B$

The voltage gain of the amplifier is

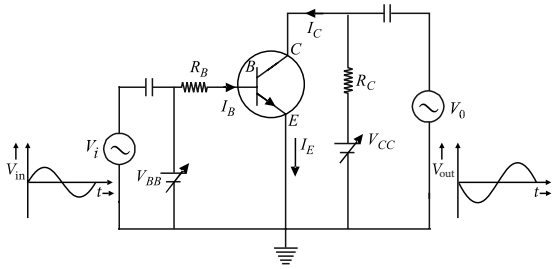
$$A_v = \frac{v_0}{v_i} = \frac{\Delta V_{CE}}{r\Delta I_B} = -\frac{\beta_{ac} R_L}{r}$$

The negative sign represents that output voltage is opposite with phase with the input voltage.

81. (a) *Refer to answer 74.*

(b) *Refer to answer 80.*

82.



CE amplifier with ***n-p-n*** transistor

Condition : The transistor must be operated close to the centre of its active region.

Alternatively : The base emitter junction of the transistor must be (suitably) forward biased and the collector emitter junction must be (suitably) reverse biased.

83. (i) Dynamic output resistance is the slope of $V_{CE} - I_C$ Graph

$$R_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}} = \frac{12-8}{(3.6-3.4)\times 10^{-3}}$$

$$= \frac{4}{0.2\times 10^{-3}} = 20\ \text{k}\Omega$$

(ii) $\beta_{dc} = \dfrac{I_C}{I_B} = \dfrac{3.5\ \text{mA}}{30\ \mu\text{A}} = \dfrac{3.5\times 10^{-3}}{30\times 10^{-6}}$

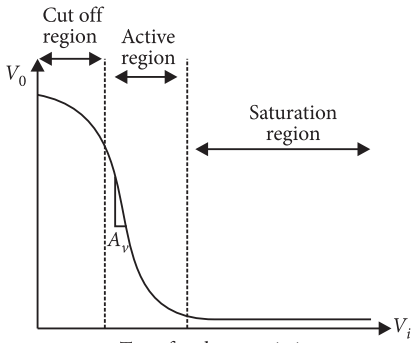
$= \dfrac{350}{3} = 116.67$

dc current gain is the ratio of output current *i.e.* I_C and input current I_B.

(iii) $\beta_{ac} = \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{(4.7-3.5)\ \text{mA}}{(40-30)\ \mu\text{A}} = \dfrac{1.2\times 10^{-3}}{10\times 10^{-6}} = 120$

ac current gain is the ratio of change in output current I_C to the change in input current I_B.

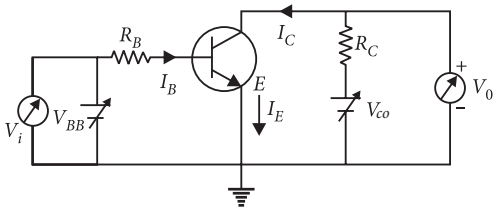
84. Transfer characteristics : The graph between V_0 and V_i is called the transfer characteristics of the base-biased transistor, is shown in figure.



Transfer characteristic

When the transistor is used in the cutoff or saturation state. It acts as a switch.

Transistor as a switch : The circuit diagram of transistor as a switch is shown in fig.



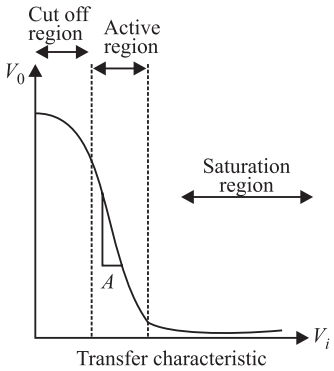
Base-biased transistor in CE configuration.

As long as V_i is low and unable to forward bias the transistor, V_0 is high (at V_{CC}). If V_i is high enough to drive the transistor into saturation, then V_0 is low, very near to zero.

When the transistor is not conducting it is said to be switched off and when it is driven into saturation it is said to be switched on. This shows that if we define low and high states as below and above

certain voltage levels corresponding to cut-off and saturation of the transistor, then we can say that a low input switches the transistor off and a high input switches it on.

85.



In active region the transistor is used as an amplifier.

(i) Input Resistance : It is the ratio of change in emitter base voltage (ΔV_{BE}) to the corresponding change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}) *i.e.*,

$$\text{Input resistance } r_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}=\text{ constant}}$$

The input resistance is very small, of the order of a few ohms, because a small change in V_{BE} causes a large change in I_B.

(ii) Output Resistance : It is the ratio of change in collector-emitter voltage to the corresponding change in collector current at constant base current I_B.

$$i.e.,\ r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B=\text{ constant}}$$

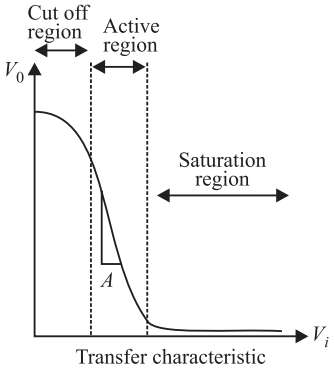
The output resistance is very high, of the order of several-tens kilo ohm because a large change in collector-emitter voltage causes a very small change in collector current.

(iii) Current amplification factor of a transistor : The current gain β is defined as the ratio of change in collector current to the change in base current for constant value of collector voltage in common emitter configuration *i.e.*,

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_C=\text{ constant}}$$

The value of β ranges from 20 to 200.

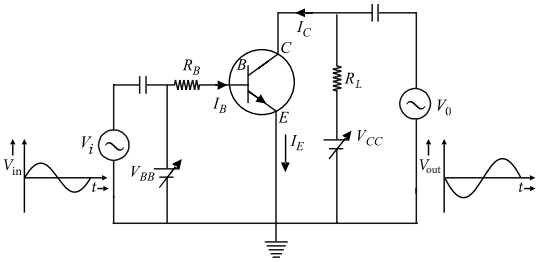
86. (i) Transfer characteristics : The graph between V_0 and V_i is called the transfer characteristics of the base-biased transfer in CE configuration as shown in figure.



(a) When the transistor is used in the cutoff or saturation state, it acts as a switch.

(b) The transistor acts as amplifier in the active region.

(ii) The circuit details for using an *n-p-n* transistor as common emitter amplifier are shown in the figure.



CE amplifier with ***n***-*p*-*n* transistor

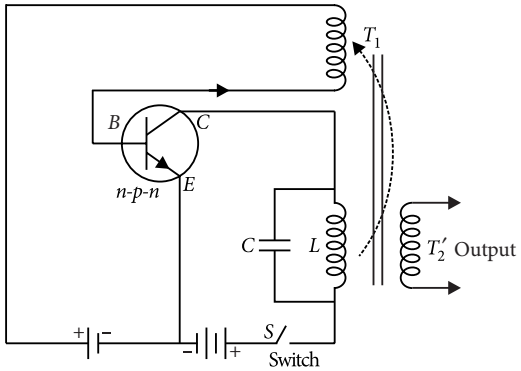
When no a.c. signal is applied, the potential difference V_{CE} between the collector and the emitter, is given by

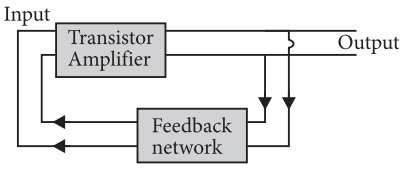
$V_{CE} = V_{CC} - I_C R_L$ ... (i)

Phase relationship between input and output signals : When an a.c. signal is fed to the input circuit, its positive half cycle increases the forward bias of the circuit which in turn, increases the emitter current and hence the collector current. The increase in collector current increases the potential drop across R_L. Which makes the output voltage V_{CE} less positive or more negative. So as the input signal goes through its positive half cycle, the amplified output signal goes through a negative half cycle. Similarly, as the input signal goes through its negative hay cycle, the amplified output signal goes through its positive half cycle. Hence in a common emitter amplifier the input and output voltages are 180° out of phase or in opposite phase.

87. *Refer to answer 86(ii)*

88. Transistor as an oscillator : In an oscillator, the output at a desired frequency is obtained without applying any external input voltage. The common emitter *n-p-n* transistor as an oscillator is shown in the following figure. *A* variable capacitor *C* of suitable range is connected in parallel to coil *L* to give the variation in frequency.





Oscillator action :

As in an amplifier, the base-emitter junction is forward biased while the base collector junction is reverse biased. When the switch *S* is put on, a surge of collector, current flows in the coil T_2. The inductive coupling between coil T_2 and T_1 cause a current to flow in the emitter circuit *i.e.*, feedback from input to output. As a result of positive feedback, the collector current reaches at maximum. When there will be no further feedback from T_2 to T_1, the emitter current begins to fall and collector current decreases. Therefore, the transistor has reverted back to its original state. The whole process now repeats itself.

The resonance frequency (f) of the oscillator is given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The tank of tuned circuit is connected in the oscillator side. Hence it is known as tuned collector oscillator.

89. *Refer to answer 86(ii).*

The phase difference between the input signal and output signal is 180°. Common emitter amplifier is preferred because –

a. Power gain is very high.
b. Voltage gain is greater.

90. (i) The values displayed by Gautam's grandmother are :

(a) Curiosity (b) Awareness

The inculcation of these values in students can be promoted by positive mental state, improvement in motives and healthy supportive environment.

(ii) The function of an amplifier to increase the amplitude of variation of alternating voltage or current or power.

(iii) Transistor is the basic electronic device used in the amplifier.

91. (a) Device $X \rightarrow C_E$ Amplifier

Power gain A_p of the transistor may be expressed as :

Ac power gain (A_p) = Current gain (β_{ac}) × Voltage gain (A_v)

$$A_p = \beta_{ac}^2 \cdot \frac{R_L}{R}$$

As power is always positive, hence power gain A_p is always positive.

Refer to answer 80.

(b) *Refer to answer 74.*

92. (a) Every transistor consists of three regions.

(i) Emitter is the section on one side of transistor, that supplies charge carriers. It is heavily doped and of modrate size it is always forward biased with respect to base, so that it can supply a large number of charge carriers to the base.

(ii) Collector is the section on the other side of transistor, that collects the charge carriers. It is moderately doped but large in size and is always kept in reverse bias with respect to base.

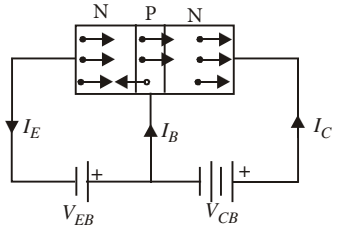
(iii) Base is the middle section of transistor, that forms two *p-n* junctions with emitter and collector. It is very thin and lightly doped so as to pass most of the emitter injected charge carriers to the collector.

(b) A transistor will be in active state if the input circuit is forward biased and the output circuit is reverse biased.

(c) *Refer to answer 80.*

93. *Refer to answer 88.*

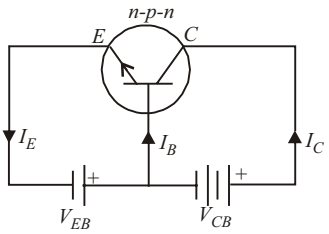
94. (a)



As soon as an electron from the emitter combines with a hole in the base region, an electron leaves the negative terminal of the battery V_{EB} and at the same time the positive terminal of battery V_{EB} receives an electron from the base. This sets a base current I_B. Similarly, corresponding to each electron that goes from collector to positive terminal of V_{CB}, an electron enters the emitter from negative terminal of V_{EB}. Hence

$I_E = I_B + I_C \quad [I_B << I_C]$

Here I_B is a small fraction of I_C depending on the shape of transistor, thickness of base, doping levels, bias voltage, etc.



(b) *Refer to answer 80.*

95. *Refer to answer 79.*

96. (a) Base provides the proper junction for inter-connection between emitter and collector. It is made thin and lightly doped, so the number of majority carriers is low. So less number of electrons-hole recombination take place and a large number of charge carriers emitted from the emitter is passed to the collector.

(b) *Refer to answer 79.*

97. *Refer to answer 80.*

98. (a) *Refer to answer 79.*

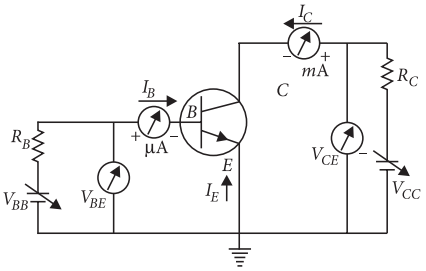
(b) *Refer to answer 84.*

99. $X \rightarrow$ Amplifier

$Y \rightarrow$ Feedback network

Refer to answer 88.

100.



Circuit arrangement for studying the input and output characteristics of n-p-n transistor in CE configuration.

Refer to answers 74 and 80.

101. *Refer to answer 88.*

102. (a) *Refer to answer 79.*

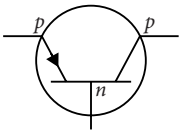
(b) *Refer to answer 88.*

103. *Refer to answer 84.*

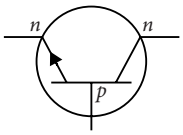
104. *Refer to answer 79.*

105. *Refer to answers 79 and 80.*

106. (i) Symbol of *p-n-p* transistor



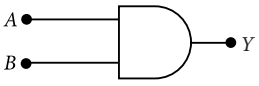
(ii) Symbol of *n-p-n* transistor



Refer to answer 96(a) and 73.

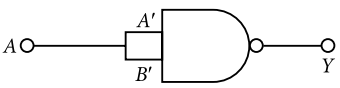
107. It is the combination of AND and NOT gates.

Logical symbol :



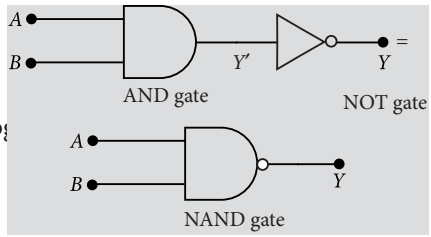
Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
1	0	1
0	1	1
1	1	0

108.



Truth table

Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
1	0	1
0	1	1
1	1	0

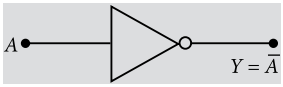


109. Lo

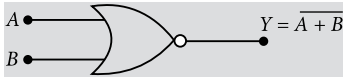
Truth table

Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

110. This logic gate is NOT gate and its symbol :



111. The gate is NOR gate and its symbol is



112. Here, R represents OR gate and S represents AND gate.

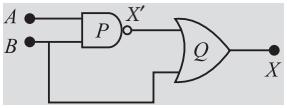
The output Y of the given combination of gates

$Y = Y'A$

Truth table for the given combination

A	B	$Y' = A + B$	$Y = Y'A$
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

113. Here, P represents NAND gate and Q represents OR gate.



The output X of the given combination of gates

$X = (B + X')$

Truth table for given combination

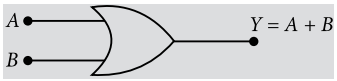
A	B	$X' = \overline{AB}$	$X = (B + X')$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	1

114. Truth table for the given circuit

A	B	Y_1	Y_2	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

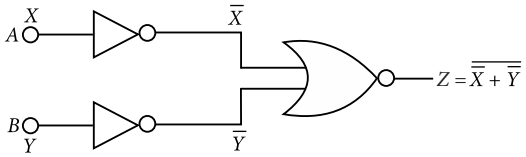
From the table, we can conclude that the given circuit represents an OR gate.

The logic symbol and truth table for an OR gate is given below.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

115. Logic circuit :

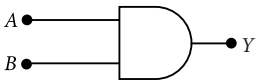


X	Y	$\overline{X}$	$\overline{Y}$	$\overline{X} + \overline{Y}$	$Z = \overline{\overline{X} + \overline{Y}}$
0	1	1	0	1	0
1	0	0	1	1	0
0	0	1	1	1	0
1	1	0	0	0	1

The equivalent gate of given circuit is AND gate.

116. It represent NAND gate.

Logic symbol :



Truth table

Input		Output
A	B	$Y = \overline{A \cdot B}$
0	0	1
1	0	1
0	1	1
1	1	0

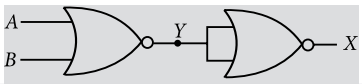
117. Here both the input terminals A and B are short circuited.

Truth table

Input		Output
A	B	$Y = \overline{A' \cdot B'}$
0	0	0
0	1	1
1	0	1
1	1	1

So, the equivalent gate is OR gate.

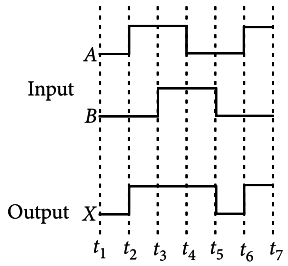
118.



Boolean expression of this combination is,

$Y = \overline{A + B}$ and $X = \overline{Y} = \overline{\overline{A + B}} = A + B$

Therefore, the given logic circuit acts as OR gate. Hence, output is high when both or one of them is high.



Accordingly the waveform of output is shown in figure.

119. It is a logic circuit in which X is NAND gate and Y is NOT gate.

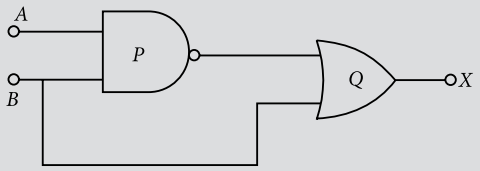
Truth table for given circuit :

A	B	$C = \overline{A \cdot B}$	$Z = \overline{C}$
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

The combination formed is a AND gate.

$\therefore \quad Z = A \cdot B$

120. (i)



Gate P is a NAND gate, and gate Q is an OR gate.

(ii) Boolean expression for the above logic circuit is

$X = \overline{A \cdot B} + B = \overline{A} + \overline{B} + B = \overline{A} + 1$

$X = 1$ [using boolean identities]

Thus output at X is going to be 1 for all the possible inputs at A and B.

121. $Y = \overline{\overline{A + B}} = A + B$

The equivalent gate is OR gate.

Truth table for given circuit :

Input		Output
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

122. For the NAND gate, the Boolean expression is

$Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

For the given wave form, we have the following values for A, B and Y.

For time $t < t_1$, $A = 1, B = 1 \quad \therefore \quad Y = 0 + 0 = 0$

For t_1 to t_2, $A = 0, B = 0 \quad \therefore \quad Y = 1 + 1 = 1$

For t_2 to t_3, $A = 0, B = 1 \quad \therefore \quad Y = 1 + 0 = 1$

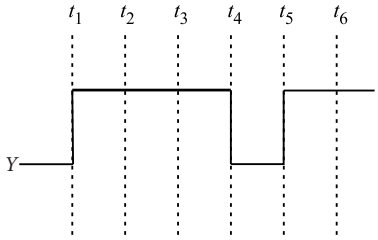
For t_3 to t_4, $A = 1, B = 0 \quad \therefore \quad Y = 0 + 1 = 1$

For t_4 to t_5, $A = 1, B = 1 \quad \therefore \quad Y = 0 + 0 = 0$

For t_5 to t_6, $A = 0, B = 0 \quad \therefore \quad Y = 1 + 1 = 1$

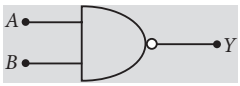
For $t_6 > t_7$, $A = 0, B = 1 \quad \therefore \quad Y = 1 + 0 = 1$

Thus, the wave form for output Y is given as,



123. The gate P is AND gate and gate Q is a NOT gate. Equivalent gate representing this circuit is NAND gate.

Logic symbol of NAND gate :



Truth table for given circuit :

A	B	X	Y
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

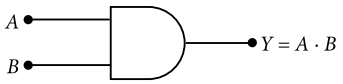
124.

$\because \quad Z = \overline{\overline{A} + \overline{B}}$

$\therefore \quad Z = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$

Hence, the equivalent gate is AND gate.

Logic symbol :



Truth table :

Input		Output
A	B	Y = A · B
0	0	0
0	1	0
1	0	0
1	1	1

125. *Refer to answer 124.*

126. Output of gate (A)

$Y_1 = \overline{A}$

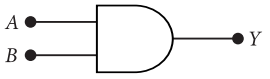
Output of gate (B)

$Y_2 = \overline{B}$

Output $Y = Y_1 + Y_2 = \overline{\overline{A} + \overline{B}}$

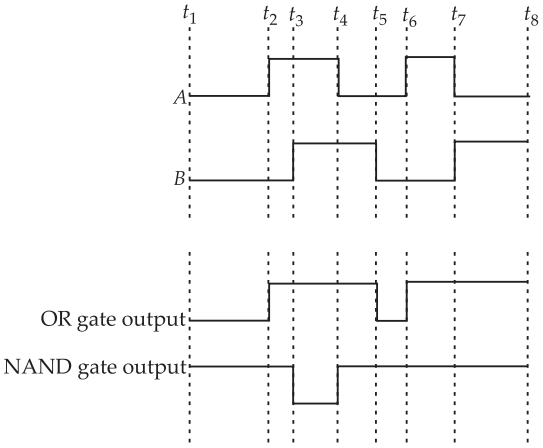
$= \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$

Thus, the complete circuit acts as AND gate. The symbol and truth table for complete circuit are given below :

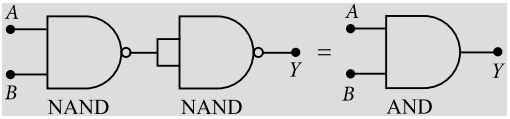


A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

127.



128. Logic gate represented by the circuit is AND gate.



Truth table :

Input		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1