Chapter 4

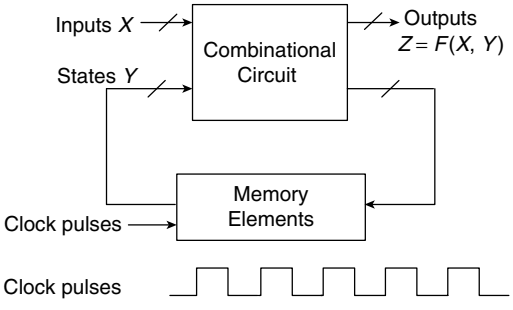
Sequential Circuits

CHAPTER HIGHLIGHTS

- *Sequential Circuits*
- *Basic Storage Elements*
- *JK Latch by using SR Latch*
- *Flip Flops*
- *Triggering of Flip Flop*
- *D Flip-flop by using other Flip Flops*
- *Counters*
- *Asynchronous Decode Counter*
- *Registers*
- *Shift Register Counters*

Sequential Circuits

In sequential circuits, the output depends on both the input and the previous history of outputs, that is, they contain memory elements.



Comparison Between Combinational and Sequential Circuits

	Combinational circuits	Sequential circuits
1.	Outputs at any time depends on the combined set of inputs applied to it simultaneously at that instant of time	Output depends on both the present input and the previous history of outputs
2.	Contains no memory element	Contains at least one memory element
3.	Easy to design due to absence of memory	Difficult to design
4.	Its performance is described by the set of output values of it.	Its performance is totally described by the set of subsequent value and set of output values.
5.	Faster in speed because all inputs are primary inputs and applied simultaneously	Slower in speed because secondary inputs are also needed which are applied after delay
6.	It needs more hardware for realization	Less hardware required
7.	It is expensive.	It is inexpensive.

Sequential circuits are of two types.

1. Clocked or Synchronized
2. Unclocked or Asynchronized

In synchronized sequential circuits, the logic circuits action is allowed to occur in synchronization with the input clock pulse from a system clock.

In asynchronized sequential circuits, the logic sequential action is allowed to occur at any time.

Basic Storage Elements

Latches and flip-flops

A storage element in digital circuit can maintain a binary state indefinitely until directed by an input signal to switch states.

Storage elements that operate with signal levels (i.e., level triggering of signal inputs) are referred to as latches. Those controlled by a clock transition (i.e., edge triggering) are flip-flops.

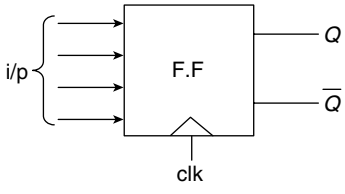
Latches and flip-flops are related because latches are basic circuits from which all flip-flops are constructed.

Latches are useful for storing binary information and for designing asynchronous sequential circuits. In practice, latches are not used in synchronous sequential circuits, and but flip–flops are used.

Flip-Flops

They are also known as bistable multivibrators. This is a basic memory element to store one bit of information 0 or 1 and is used in storage circuits, counters, shift register, and many other computer applications. It has two stable states one and zero. The high state is called set state and zero as reset.

It has two outputs, that is, one being the complement of the other, and usually designated by Q and $\bar{Q}$.



There are different types of flip-flops such as S-R flip-flop, D flip-flop, T flip-flop, J-K flip–flops, etc.

Latches

S-R Latch

The simplest latch is called S-R Latch. S-R means Set, Reset Latch. They have two outputs Q and $\bar{Q}$ and two inputs S and R, which represents set or reset signal.

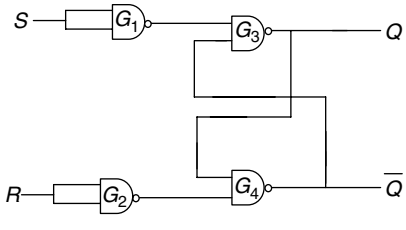


Figure shows two cross coupled gates G_3 and G_4 and inverters G_1 and G_2. Here, output of G_3 is connected to the input of G_4 and output of G_4 is applied to the input of G_3. $S = 1$, $R = 0$ output of $G_1 = 0$ and $G_2 = 1$. Since one of the input of G_3 is zero and its output will certainly one consequently both input of G_4 will be one and the output $\bar{Q} = 0$.

For $S = 1$, $R = 0$, $Q = 1$, $\bar{Q} = 0$

For $S = 0$, $R = 1$, the output will be $Q = 0$ and $\bar{Q} = 1$. The first of the input condition $S = 1$ and $R = 0$ makes $Q = 1$ which referred as the set state and the second condition $S = 0$ and $R = 1$ makes $Q = 0$ which is referred as reset state.

For $S = 0$ and $R = 0$, the output of both G_1 and G_2 will be one, and hence, there will be no change in Q and $\bar{Q}$.

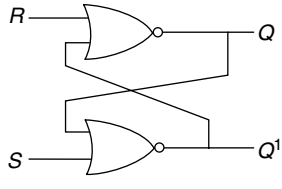
For $S = R = 1$, both the outputs Q and $\bar{Q}$ will try to become one which produce invalid results and should not be used for the above latch.

The truth table is given as follows:

Input		Output		
S	R	Q	$\bar{Q}$	State
1	0	1	0	Set
0	1	0	1	Reset
0	0	0	0	No change
1	1	x	x	Invalid

S-R Latch Using NAND/NOR Gates

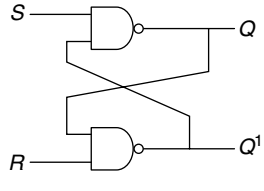
The S-R latch is circuit with two cross coupled NOR gates or two cross coupled NAND gates. Two inputs labelled S for set and R for reset. Latch will have two outputs Q and Q^1, Q – output state in normal form, Q^1– output state in complemented form.



Logic diagram for S-R latch

S	R	Q_{n+1}	Q^1_{n+1}
0	0	Q_n	Q^1_n (No change)
0	1	0	1 (Reset)
1	0	1	0 (Set)
1	1	0	0 (Invalid)

$\bar{S}$–$\bar{R}$ Latch



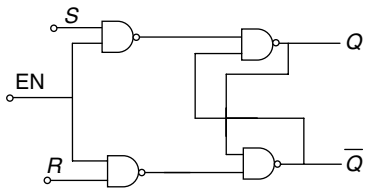
Truth table is given below.

S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	1	1	(Invalid)
0	1	1	0	(set)
1	0	0	1	(reset)
1	1	Q_n	Q^1_n	(No change)

$\bar{S}$ $\bar{R}$ Latch is active low S-R latch

S-R Latch with Control Input

The working of gated S-R latch is exactly the same as S-R Latch when the EN pulse is present. When the EN pulse is not present, (EN pulse = 0) the gates G_1 and G_2 are inhibited and will not responds to the input.

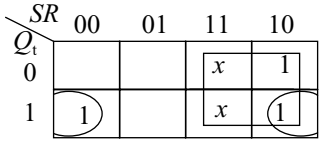


Characteristic table of S-R latch shows the operation of Latch in tabular form. Q_t stands as the binary state of the latch before the application of latch pulse and referred to as the present state. The S and R columns give the possible values of the inputs and Q_{t+1} is the state of the latch after the application of a single pulse, referred to as next stage. EN input is not included in the characteristic table.

Characteristic table for S-R latch is given below.

Q_t	S	R	Q_{t+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Characteristic equation of the latch is derived from the *k*-map



Therefore,

$$Q_{t+1} = S + \bar{R}Q_t$$

This equation specifies the value of the state as a function of the present state and the inputs.

Preset and Clear Inputs

For the latch/flip-flop, when the power is switched ON, the state of the circuit is uncertain. It can be either $Q = 0$(reset) or $Q = 1$ (set) state.

In many applications, it is desired to set or reset the circuit, so that initial state of the circuit will be known. This is accomplished by using the asynchronous inputs referred as preset (Pr) and clear (Clr) inputs.

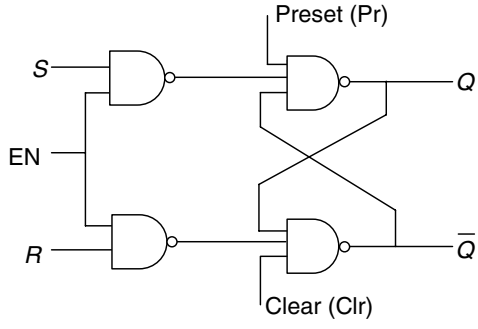
These inputs can be applied any time and are not synchronized with EN input/Clk input.

If Pr = Clr = 1, the circuits operates as of S–R latch explained previously.

If Pr = 0, Clr = 1, the output Q will become 1, which in turn changes $\bar{Q} = 0$

If Pr = 1, Clr = 0, the output $\bar{Q}$ will becomes 1.

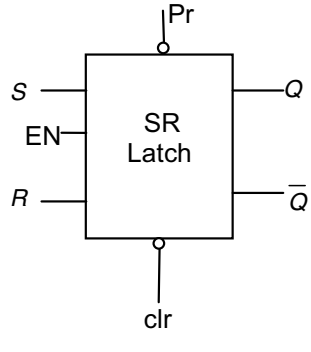
Which in turn changes $Q = 0$



S-R latch with Pr and Clr inputs

If Pr = Clr = 0, both Q and $\bar{Q}$ will become 1, which is invalid case, so Pr = Clr = 0 condition must not be used. The truth table is given below.

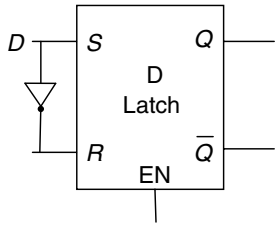
Pr	Clr	Q_{n+1}
1	1	Q – No change
0	1	1 – Set
1	0	0 – Reset
0	0	X – Invalid



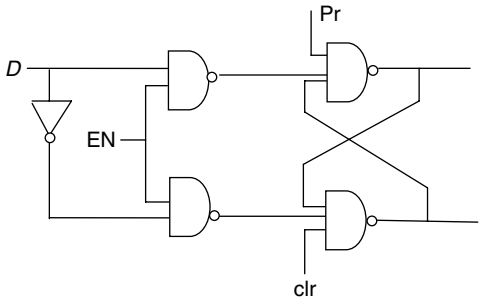
D Latch (Transparent Latch)

One way to eliminate the invalid condition of S-R latch (When $S = R = 1$) is to ensure that inputs S and R are never equal to 1 at the same time.

By connecting a NOT gate between S and R inputs. that is, complement of S will be given to R, we can form D latch as shown in block diagram.



Block diagram for D latch



Logic diagram for D latch

EN	D	Q_{n+1}
0	X	Q_n – No change (Disabled)
1	0	0 – Reset state
1	1	1 – Set state

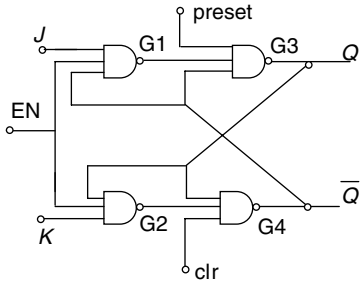
When EN = 0, the circuit will be disabled and input D will not have only effect on output, and output will be same as previous state.

When EN = 1, $D = 0$, that is, $S = 0$, $R = 1$ which makes output $Q = 0$, and $\bar{Q} = 1$, (reset state)

When EN = 1, $D = 1$, that is, $S = 1$, $R = 0$ which makes output $Q = 1$, and $\bar{Q} = 0$ (Set state)

J-K Latch

The function of J-K latch is identical to that of S-R latch except that it has no invalid state as that of S-R latch where $S = R = 1$. In this case, the state of the output is changed as complement of previous state.



J-K latch using S-R latch

EN	J	K	Q_{t+1}	
1	0	0	Q_t	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\bar{Q}_t$	Toggle
0	x	x	Q_t	No change

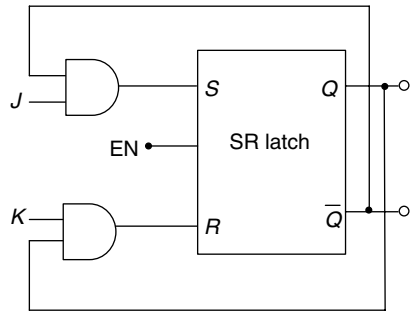
J-K Latch by using S-R Latch

The uncertainity of S-R flip-flop (When $S = 1$, $R = 1$) can be eliminated by converting into J-K latch.

The data inputs J and K which are ANDed with $\bar{Q}$ and Q, respectively, to obtain S and R inputs.

$$S = J.\ \bar{Q}$$

$$\because\ R = K.\ Q$$



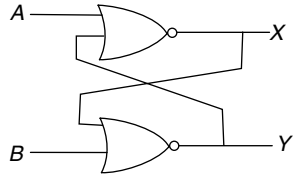
J-K latch using S-R latch

J	K	S	R	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	0	Q_n	$\tilde{Q}_n$ – No change
0	1	0	Q_n	0	1 – Reset
1	0	$\tilde{Q}_n$	0	1	0 – Set
1	1	$\bar{Q}_n$	Q_n	$\tilde{Q}_n$	Q_n – Toggle

Solved Examples

Example 1

The following binary values were applied to the A and B inputs of the NOR gate latch shown in the figure, in the sequence indicated below. $A = 1$, $B = 0$; $A = 1$, $B = 1$; $A = 0$, $B = 0$. The corresponding stable X, Y outputs will be



(A) 10, 01, 10, or 01 (B) 11, 00, 10
(C) 01, 00, 10, or 01 (D) 10, 11, 10, or 01

Solution

Given circuit is R-S latch with NOR gates.

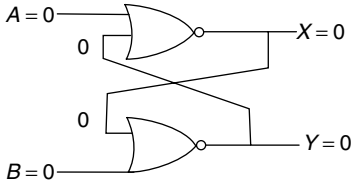
By comparing with R-S latch $A = R$, $B = S$, and $X = Q$, $Y = \bar{Q}$, so from truth table of R-S latch

S/B	R/A	Q/X	$\bar{Q}$/Y
0	1	0	1 Reset
1	1	0	0 (Invalid)
0	0	1	0 (Same as previous state)
1	0	0	1

After invalid case $S = 1$, $R = 1$, i.e, $A = B = 1$,
The output $Q = 0$, $\bar{Q} = 0$, i.e, $X = Y = 0$
By applying $A = 0$, $B = 0$

The output X becomes $\overline{(0+0)} = 1$ and which in turn changes

$$Y = \overline{(B+X)} = \overline{(0+1)} = 0$$



(or) the output Y becomes $\overline{(0+0)} = 1$ and which in turn changes $X = \overline{(Y+A)} = \overline{(0+1)} = 0$

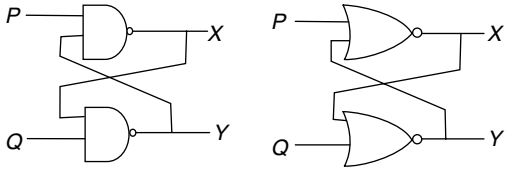
So, output (X, Y) cannot be predicted after the invalid condition

So $X = 0$, $Y = 1$ or $X = 1$, $Y = 0$

Hence, the correct option is (C).

Example 2

Refer to the NAND and NOR latches shown in the figure the inputs (P, Q) for both latches are first made (1, 0) and then after a few seconds, made (0, 0). The corresponding stable outputs (X, Y) are as follows:



(A) NAND: first (0, 1), then (0, 1); NOR: first (1, 0), then (1, 0)
(B) NAND: first (0, 1), then (1, 1); NOR: first (0, 1), then (0, 1)
(C) NAND: first (1, 0), then (0, 0); NOR: first (1, 0), then (1, 0)
(D) NAND: first (1, 0), then (1, 0); NOR: first (1, 0), then (1, 1)

Solution

From the truth table of S-R latch and $\overline{S}\ \overline{R}$ latches

S-R latch with NOR gates.

For $(P, Q) = (1, 0) = (R, S)$ output $(X, Y) = \left(Q, \overline{Q}\right) = (0, 1)$

Then (P, Q) are made (0, 0). That is, $(R, S) = (0, 0)$ which results in no change at output

So $(X, Y) = \left(Q, \overline{Q}\right) = (0, 1)$

S-R latch with NAND gates

For $(P, Q) = (1, 0) = (S, R)$ output $(X, Y) = \left(Q, \overline{Q}\right) = (0, 1)$

Then, (P, Q) are made (0, 0), i.e, $(S, R) = (0, 0)$ which is invalid conditions for $\overline{S}\ \overline{R}$ latch

So $(X, Y) = \left(Q, \overline{Q}\right) = (1, 1)$

Hence, the correct option is (B).

Race Around Condition

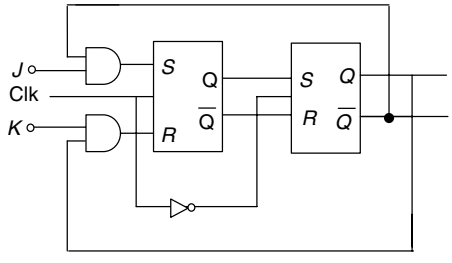
The difficulties of both inputs ($S = R = 1$) being not allowed in an S-R latch is eliminated in J-K latch by using the feedback connection from the output to the input of the gate G_1 and G_2. In a normal J-K latch, if $J = K = 1$ and $Q = 0$ and enable signal is applied without RC differentiator, after a time interval Δt (the propagation delay through two NAND gate in series), the output will change to $Q = 1$. Now, we have $J = K = 1$ and $Q = 1$, and after another time interval of Δt, the output will change back to $Q = 0$. Hence, for the duration of (t_p) of the enable signal, the output will oscillates back and forth between 0 and one. At the end of the enable signal, the value of Q is uncertain. This situation is referred as race around condition.

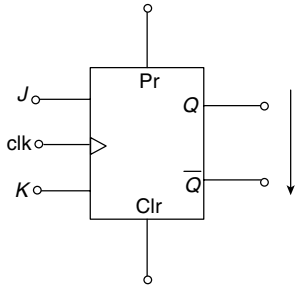
The race around condition can be avoided if enable time period $t_p < \Delta t$, but it may be difficult to satisfy this condition, because of very small propagation delays in integrated circuits (ICs). To solve this problem, the enable signals are converted to narrows spike using RC differentiator circuit having a short-time constant. Its output will be high during the high transmission time of the enable. Another method to avoid this problem is master slave J-K flip-flop.

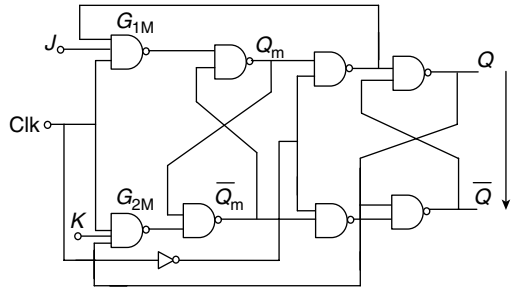
Flip-Flops

Master Slave J-K Flip-Flop

This is a cascade of two S-R latches with feedback from the output of the second S-R latch to the inputs of the first as shown in figure below.





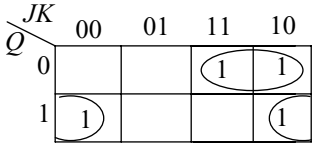


Positive clock pulse is applied to the first latch and the clock pulse will be inverted before its arrival at the second latch. When clk = 1, the first latch is enabled and the outputs Q_m and $\overline{Q}_m$ responds to the inputs J and K, according to

the truth table of J-K latch. At this time, the second latch is inhibited because its clock is low. ($\overline{clk}$ = 0). When the clock goes low (clk = 0), the first latch is inhibited and the second is enabled. Therefore, the outputs Q and $\overline{Q}$ follow the outputs Q_m and $\overline{Q_m}$ respectively. Since the second latch simply follows the first one, it is referred to as slave and the first one as the master. Hence, this configuration is known as master slave J-K flip-flop. In this circuit, the input to the gate G_{1m} and G_{2m} does not change, during the clock pulse levels. Therefore, the race around condition does not exist.

State table/Characteristic table

Clk	J	K	Q_t	Q_{t+1}	
↓	0	0	0	0	Q_t
↓	0	0	1	1	
↓	1	0	0	1	1
↓	1	0	1	1	
↓	0	1	0	0	0
↓	0	1	1	0	
↓	1	1	0	1	$\overline{Q}_t$
↓	1	1	1	0	



$$Q_{t+1} = J\overline{Q}_t + Q_t\overline{K}$$

Flip-Flop Switching Time

In designing circuits with flip-flop, the following parameters are important.

(1) Set-up time
(2) Hold time
(3) Propagation delay

(1) Set-up time

The minimum amount of time required for the data input to be present before the clock arrived.

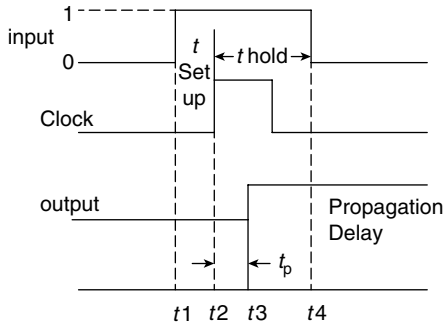
(2) Hold time

The minimum amount of time that the data input to be present after the clock trigger arrived.

(3) Propagation delay

The amount of time it takes for the output to change states after an input trigger.

For example, t set-up = 50 ms and t hold = 5 ms, the data bit has to be the input at least 50 ms before the clock bit arrives and hold at least 5 ms after the clock edge.

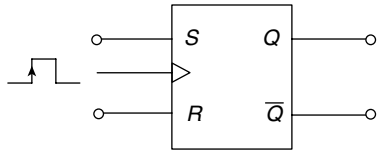


Triggering of Flip-Flop

The flip-flop can be triggered to set or reset either at one of the edges of the clock pulse. There are three types of triggering as described below.

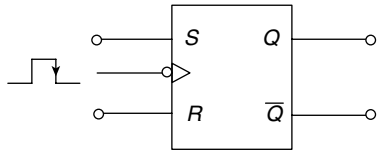
Positive Edge Triggering Flip-Flop

These set or reset at the positive (rising or leading) edge of the clock pulse depending upon the state of input (i/p) signal and output (o/p) remain steady for one clock period. Positive edge triggering is indicated by an arrow head at the clock terminal of the flip-flop.



Negative Edge Triggered Flip-Flop

There are flip-flops those in which state transmissions take place only at the negative edge (falling or trailing) of the clock signal. Negative edge triggering is indicated by arrow head with bubble at the clock terminal.



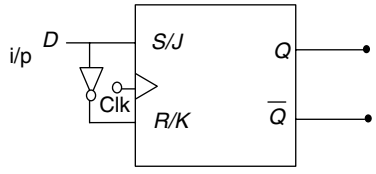
Level Triggering

Level triggering means the specified action occurs based on the steady-state value of the input. That is, when a certain level is reached (0 or 1) the output will change states level triggering will be used in latches.

D Flip-Flop

It receives the designation from its ability to hold data into its internal storage. An S-R/J-K flip-flop has two inputs. It requires two inputs S/J and R/K to store 1 bit. This is a serious disadvantage in many application to overcome the difficulty D flip-flop has been developed which has only one

input line. A D flip-flop can be realized using a S-R/J-K as shown in the figure below.



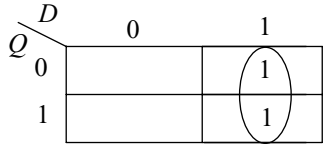
Truth table is given as follows:

Clk	D	Q_{t+1}
↕	X	Q_t
↑	0	0
↑	1	1

There is no raising problem with D flip-flop. High or 1 state will set the flip-flop and a low or 0 state will reset the flip-flop. The presence of inverter at the input ensure that *S*/*J* and *R*/*K* inputs will always be in the opposite state.

Characteristic table of D flip-flop

Q_t	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

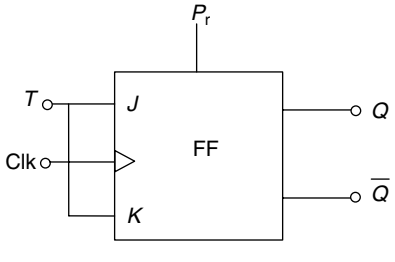


$$Q_{t+1} = D$$

From the characteristic table of D flip-flop, the next state of the flip-flop is independent of the present state since $Q_{t+1} = D$ whether $Q_t = 0$ or 1.

T Flip-Flop

In a J-K flip–flop, if $J = K = 1$, the resulting flip-flop is referred as a T flip-flop.



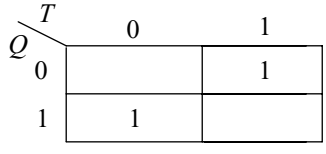
Truth table

CIK	T	Q_{n+1}
↑	0	Q_n
↑	1	$\overline{Q_n}$
↕	x	Q_n

If $T = 1$, it acts as a toggle switch for every clk pulse with high input, the Q changes to its opposite state.

Characteristic table is as follows:

Q_t	T	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0
1	0	1



$$Q_{t+1} = T\,\overline{Q}_t + Q_t\,\overline{T}$$

Excitation Table of Flip-Flops

The truth table of flip-flop is also referred as the characteristic table, which specifies the operational characteristic of flip-flop.

Sometimes we come across situations, in which present state and the next state of the circuit are known, and we have to find the input conditions that must prevail to cause the desired transition of the state.

Consider initially J-K flip-flop, the output $Q_n = 1$, $\overline{Q}_n = 0$, after clock pulse, it changed to $Q_{n+1} = 0$, $\overline{Q}_{n+1} = 1$,

The input conditions which made this transition can be as follows:

Toggle – for $J = 1$, $K = 1$, $Q_{n+1} = \overline{Q}_n$

Or Reset – for $J = 0$, $K = 1$, $Q_{n+1} = 0$, $\overline{Q}_{n+1} = 1$

From the above conditions, we can conclude that for transition $Q_n = 1$ to $Q_{n+1} = 0$ occurs when $J = 0$ (or) 1 (do not care) and $K = 1$.

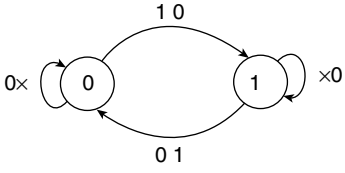
Similarly input conditions can be found out for all possible situations.

Present state	Next state	S-R Flip-flop		J-K Flip-flop		T Flip-flop	D Flip-flop
Q_n	Q_{n+1}	S	R	J	K	T	D
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	1	0
1	1	×	0	×	0	0	1

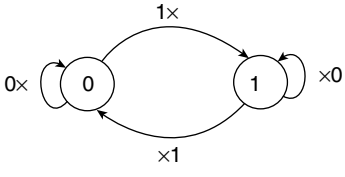
These excitation tables are useful in the design of synchronous circuits.

State Diagrams of Flip-Flops

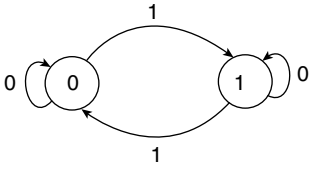
State diagram is a directed graph with nodes connected with directed arcs. State of the circuit is represented by the node, and the directed arcs represent the state transitions, from present state (node) to next state (node) at the occurrence of clock pulse.



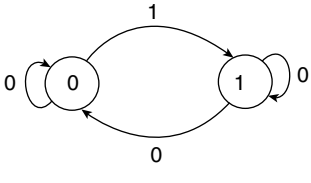
State diagram of S-R flip-flop



State diagram of J-K flip–flop



State diagram of T flip–flop



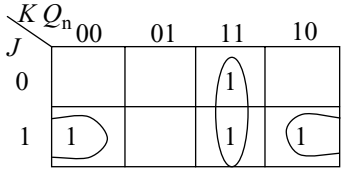
State diagram of D flip-flop

Conversion of One Flip-Flop to Other Flip-Flop

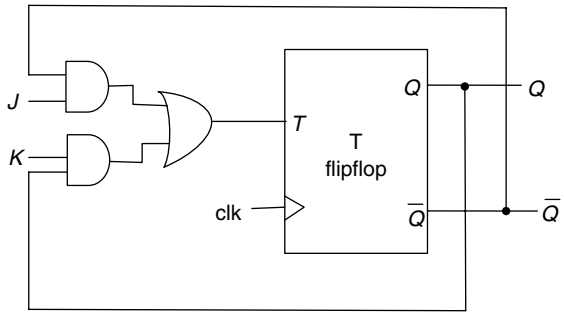
The conversion of T flip-flop to J-K flip-flop

(1) write the characteristic table of required flip-flop (here J-K)
(2) write the excitation table of available or given flip-flop (here T)
(3) solve for inputs of given flip-flop in terms of required flip-flop inputs and output.
J-K flip-flop characteristic T flip-flop excitation table.

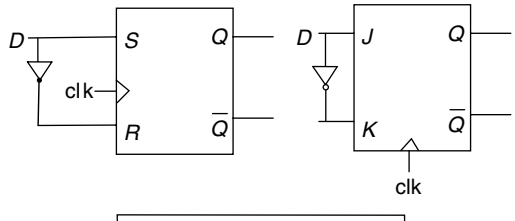
J-K flip-flop characteristic table				
		T flip-flop excitation table		
J	**K**	Q_n	Q_{n+1}	**T**
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

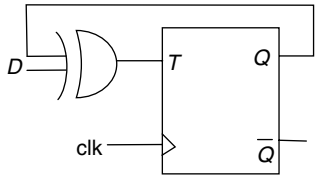


$$T = J\,\overline{Q}_n + K\,Q_n$$

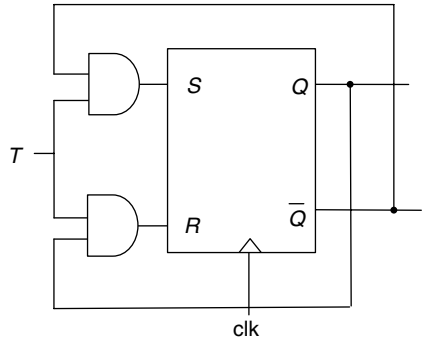


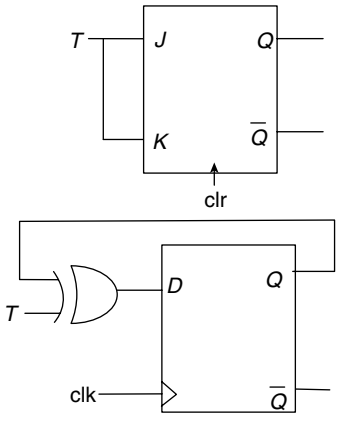
D Flip-flop by using other flip-flops





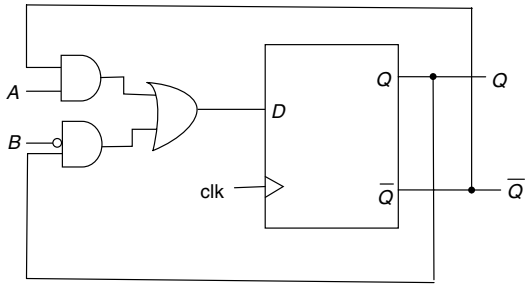
T Flip-flop by using other flip-flops





Example 3

A sequential circuit using D flip-flop and logic gates is shown in the figure, where A and B are inputs and Q is output.



The circuit is

(A) S-R flip-flop with inputs $A = S, B = R$

(B) S-R flip-flop with inputs $A = \overline{R}, B = S$

(C) J-K flip-flops with inputs $A = J, B = K$

(D) J-K flip-flop with inputs $A = K, B = \overline{J}$

Solution

The characteristic equation of D flip-flop is

$$Q_{n+1} = D$$

Here, input $D = A\overline{Q}_n + \overline{B}Q_n$

So output $Q_{n+1} = A\overline{Q}_n + \overline{B}Q_n$

By comparing this equation with characteristic equation of J-K

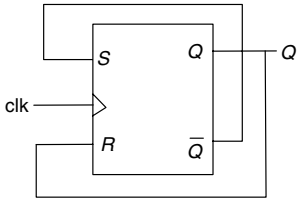
$$Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

If $A = J, B = K$, then this circuit works like J-K flip-flop.

Hence, the correct option is (C).

Example 4

The input Clk frequency for the flip-flop given is 10 KHZ, then the frequency of Q will be



(A) 10KHz (B) 5KHz (C) 20KHz (D) 2.5KHz

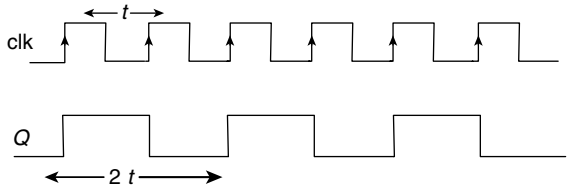
Solution

Form circuit, we can say $S = \overline{Q}_n$, $R = Q_n$.

If initially $(Q_n, \overline{Q}_n) = (0, 1)$, then inputs $(S, R) = (1, 0)$, by applying clk pulse $(Q_{n+1}\ \overline{Q}_{n+1})$ becomes (1, 0)……..

Clk	Q_n	$\overline{Q}_n$	S	R	Q_{n+1}	$\overline{Q}_{n+1}$
1	0	1	1	0	1	0
2	1	0	0	1	0	1
3	0	1	1	0	1	0
4	1	0	0	1	0	1

The output Q_{n+1} toggles for every clock pulse.

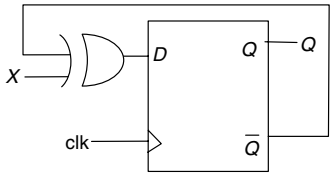


So frequency of $Q = \dfrac{1}{2t} = \dfrac{f}{2} = \dfrac{10}{2} = 5$ KHz

Hence, the correct option is (B).

Example 5

For the D flip-flop shown, if initially Q_n is set, then what is the output state Q_{n+1} for $X = 0$, and for $X = 1$



(A) 0, 0 (B) 0, 1 (C) 1, 0 (D) 1, 1

Solution

The characteristic equation of D is $Q_{n+1} = D$

Here $D = X \oplus \overline{Q_n}$

So $Q_{n+1} = X \oplus \overline{Q_n}$

We have $Q_n = 1$ (Q_n is set) for $X = 0$

$Q_{n+1} = 0 \oplus 0 = 0$

We have $Q_n = 1$ (Q_n is set), for $X = 1$

$Q_{n+1} = 1 \oplus 0 = 1$

Hence, the correct option is (B).

Applications of Flip-Flops

1. Data storage: A group of flip-flops connected in series/parallel is called a register, to store a data of N bits, N flip-flops are required. Data can be stored in parallel or serial order. Similarly, serial to parallel conversion, and parallel to serial conversion can be done by using registers.

2. Counting: A number of flip-flops can be connected in a particular fashion to count the pulses applied (clk) electronically. One flip-flop can count 2 clk pulses, two flip-flops can count up to $2^2 = 4$ pulses, and similarly, n flip-flops can count up to 2^n pulses. Flip-flops may be used to count up/down.
3. Frequency division: Flip-flops may be used to divide input signal frequency by any number. A single flip-flop may be used to divide the input frequency by 2. Similarly, n flip-flops may be used to divide the input frequency by 2^n. Output of a mod – n counter (i.e., which counts n states) will divide input frequency by n.

Counters

Digital counters consist of a number of flip-flops. Their function is to count the number of clock pulses arriving at its clock input.

Counter Classification

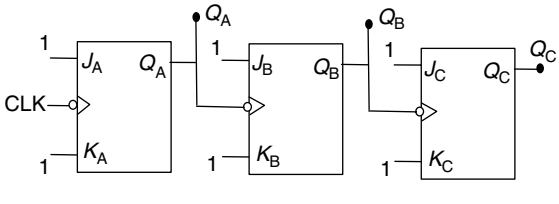
Counters are classified according to their operational characteristic. Some of these characteristics include the following:

(1) Counter triggering techniques
(2) Frequency division characteristic
(3) Counter modulus
(4) Asynchronous or synchronous

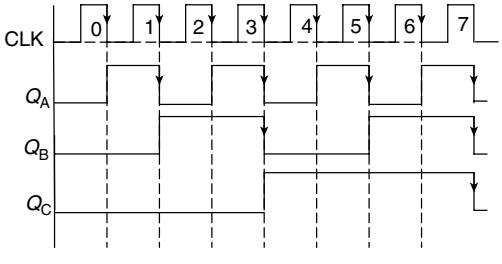
In a synchronous counter, all flip-flops are clocked simultaneously. In asynchronous counter, the flip-flops are not clocked simultaneously. Each flip-flop is triggered by the previous flip-flop.

Asynchronous Counters (Ripple Counters)

Asynchronous counters do not have a common clock that controls all the flip-flop stages. The control clock is input to the first stage. The clock for each stage subsequent is obtained from the flip-flop of the prior stages. Let us analyse the 3-bit counter and its corresponding wave form diagram shown below.



Timing Diagrams



- The counter has three flip-flops and three output bits, and therefore, it is a three-stage counter.
- The input clock does not trigger the three flip-flops, and therefore, it is an asynchronous counter.
- The J and K inputs are tied together as kept high. So they are considered to be toggle flip-flops.
- The flip-flops are negative edge triggered.
- The wave form analysis reveals that Q_A is the LSB and that its frequency is 1/2 the input clock frequency. Furthermore, Q_c is the MSB and its frequency is 1/8 the input clock frequency.
- The count sequence is 000, 001, 010, 011, 100, 101, 110, 111 where the LSB is Q_A. Thus, it is MOD-8 binary up counter.
- Asynchronous counters are also known as ripple counters because the effect of the input clock ripples through the counter until it reaches the final stage.

The procedure of asynchronous counter design is as follows:

Step 1: Write the counting sequence
Step 2: Tabulate the values of reset signals. R for various state of counter
Step 3: Obtain the minimal expression for R and $\overline{R}$ using K-map or any other method.
Step 4: Provide a feedback such that R or $\overline{R}$ resets all the flip-flops after the desired count.

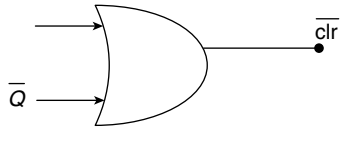
Identification of up/down counters

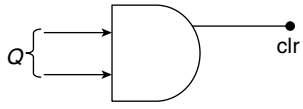
Clock triggering	Q	Type
+ve edge	$\overline{Q}$	Up
+ve edge	Q	Down
–ve edge	$\overline{Q}$	Down
–ve edge	Q	Up

Clock is negative triggering pulse, and Q is connected to next level clock, it is acting like a up counter.

Identification of GATE to clear the flip-flops

Input to the Gate	Output of the gate	Type of gate
$\overline{Q}$	$\overline{Clr}$	OR
$\overline{Q}$	Clr	NOR
Q	$\overline{Clr}$	NAND
Q	Clr	AND





Example 6

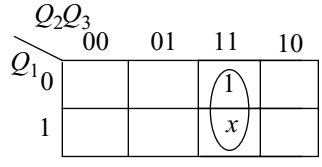
Design and implement a Mod-6 asynchronous counter using T flip-flops.

Solution

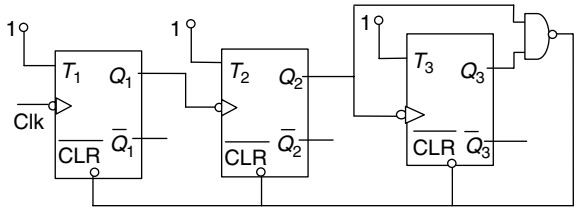
Counting sequence is: 00, 001, 010, 011, 100, 101

After pulses	States Q_3, Q_2, Q_1	Reset R
0	000	0
1	001	0
2	010	0
3	011	0
4	100	0
5	101	0
6	110	1
7	↓ ↓ ↓ 0 0 0 1 1 1	0 X

From the Truth table $R = Q_3\,Q_2$
For active Low $\overline{R}$ is used.
$\therefore R = 0$ for 000 to 101
$R = 1$ for 110
$R = X$ for 111
$\therefore$ K-map is



$\therefore R = Q_2\,Q_3$; $\therefore$ Logic diagram is as follows:

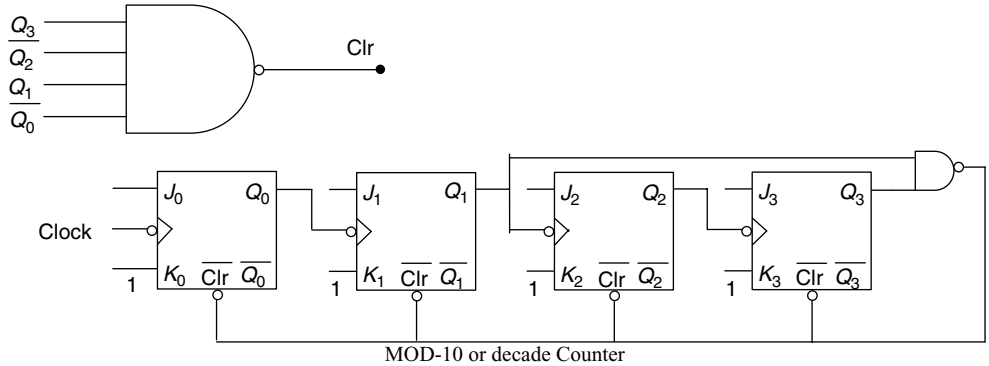


Asynchronous Decode Counter

A Ripple counter is an asynchronous sequential circuit, and clock is applying only for LSB side.

Decade ripple counter it counts from 0 to 9 for up counter.

MOD – 10 counter it counts starting from 0000 to 1001. If the NAND gate output is logic '0' at that instant the counter reset to initial state.



MOD-10 or decade Counter

To design a MOD-N counter minimum no. of flip-flops required is
$N \le 2^n$
Where $N \rightarrow$ MOD
$n \rightarrow$ No. of flip-flops
e.g., MOD – 5 counter
$5 \le 2^n$
$\therefore n = 3$

Operating, clock frequency

i) Synchronous counters:

$$f_{clk} \le \frac{1}{t_{pd}}$$

ii) Asynchronous counters:

$$f_{clk} \le \frac{1}{n\,t_{pd}}$$

Output frequency of the MOD-N counter is $\Rightarrow f_o = \frac{f_{clk}}{N}$.

Synchronous Counter

When counter is clocked such that each flip-flop in the counter is triggered at the same time, the counter is called as synchronous counter.

- Synchronous counters have the advantage of high speed and less severe decoding problems.
- Disadvantage is having more circuiting than that of asynchronous counter.

Synchronous series carry counters

For normal ring counters, to count N sequence, a total of N flip-flops are required.

Unused states in Ring Counter = $2^N - N$.

Unused states in Johnson ring counter = $2^N - 2N$.

Asynchronous counters are slower than the synchronous counters. By using synchronous series carry adders, we can design MOD-N counter with n flip-flops only.

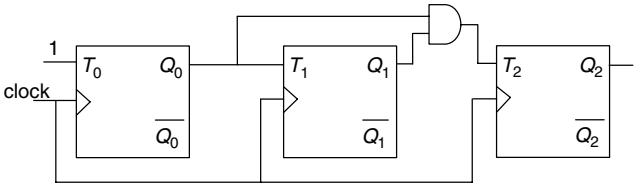
For non-binary counters, $N \le 2^n$

3-bit series carry up counter

It counts from initial state 000 to 111.

$\therefore$ MOD = $2^n = 8$ states

$\therefore$ MOD – 8



Three-bit series carry counter

$$f_{clk} \le \frac{1}{t_{pd} + (n-2)t_{pdAND}}$$

where

$t_{pd} \rightarrow$ propagation delay of each flip-flop.

$t_{pd\,AND} \rightarrow$ propagation delay of AND gate.

$n \rightarrow$ no. of flip-flops.

In this Q_o toggles for every clock pulse.

Q_1 toggles when Q_0 is 1

Q_2 toggles when o/p of AND gate is logic '1'.

NOTE

To design a synchronous series carry down counter. Connect $\overline{Q_0}$ to the next flip-flop input.

Design of Synchronous Counter

Step 1: Determine the required number of flip-flop.

Step 2: Draw the state diagram showing all possible states.

Step 3: Select the type of flip-flops to be used and write the excitation table.

Step 4: Obtain the minimal expressions for the excitations of the flip-flops using the k-maps.

Step 5: Draw a logic diagram based on the minimal expression. Let us employ these techniques to design a MOD-8 counter to count in the following.

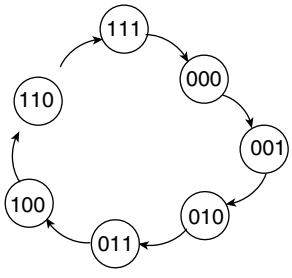
Example 7

Sequence: 0, 1, 2, 3, 4, 5, 6, and 7, Design synchronous counter by using J-K flip-flops.

Solution

Step 1: Determine the required number of flip-flops. The sequence shows a 3-bit –up counter that requires 3 flip-flops.

Step 2: Draw the state diagram

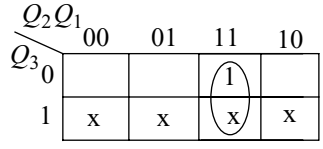


Step 3: Select the type of flip-flop to be used and write the excitation table.

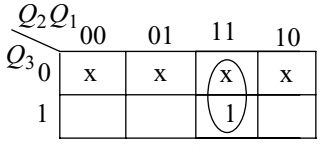
J-K flip-flop is selected and excitation table of a 3-bit up counter is.

PS			NS			Required Excitation					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

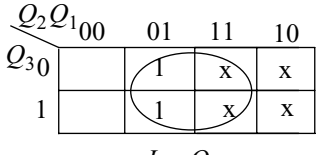
Step 4: Obtain the minimal expression using K-map



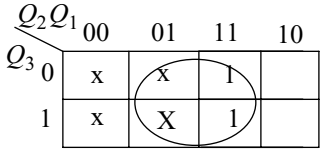
$J_3 = Q_2 Q_1$



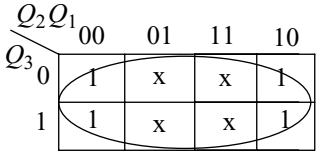
$K_3 = Q_2 Q_1$



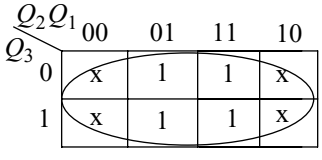
$J_2 = Q_1$



$K_3 = Q_1$

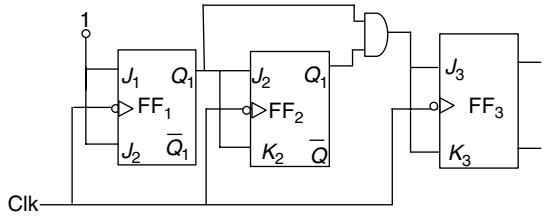


$J_1 = 1$



$K_1 = 1$

Step 5: Draw the logic diagram based on the minimal expression.



Comparison between Asynchronous Counter Synchronous Counter

	Asynchronous counter	Synchronous counter
1.	In this type of counter, flip -lops are connected in such a way that output of first flip-flop drives the clock for the next flip-flop	In this type, there is no connection between output of first flip-flop and clock input of the next flip-flop
2.	All the flip-flops are not clocked simultaneously	All the flip-flops are clocked simultaneously
3.	Logic circuit is very simple even for more number of states	Design involves complex logic circuits as number of state increases
4.	Main drawback of these counters is their low speed as the clock is propagated through number of flip-flops before it reaches last flip-flop	As clock is simultaneously given to all flip-flops. There is no problem of propagation delay. Hence, they are preferred when number of flip-flops increases in the given design.

The main drawback of ripple counters is their high delays, if propagation delay of each flip-flop is assumed as x, then to get output of the first flip-flop it takes x, that is, after x seconds, the second flip-flop will get its clock pulse from previous stage, and output of second flip-flop will be out after another x seconds, similarly the final output of last flip-flop will be after nx seconds, where n is the number of flip-flops. So the propagation delay of ripple counter is nx, which is directly proportionate to the number of flip-flops.

The maximum frequency of operation of ripple counter is inverse of delay, $f_{max} = \frac{1}{nx}$

Maximum operating frequency is the highest frequency at which a sequential circuit can be reliably triggered. If the clock frequency is above this maximum frequency, the flip-flops in the circuit cannot able to respond quickly and the operation will be unreliable.

In case of synchronous counters (synchronous circuits) as clock is applied simultaneously to all flip-flops, the output of all flip-flops change by x seconds (delay of one flip-flop) and this delay is independent of number of flip-flops used in circuit.

The maximum frequency of operation of synchronous counter is inverse of delay $f_{max} = \frac{1}{x}$

Example 8

The maximum operation frequency of a mod 64 ripple counter is 33.33 KHz, the same flip-flops are used to design a mod 32 synchronous counter, and then the maximum operating frequency of the new counter is?

(A) 400 KHz (B) 200 KHz
(C) 40 KHz (D) 500 KHz

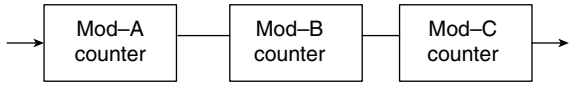
Solution

For ripple counter, $f_{max} = \frac{1}{nx}$, given is a mod 64 ripple counter, that is, 2^6 states, so $n = 6$ flip-flops are required.

$$x = \frac{1}{33.33K \times 6} = 5\,\mu S$$

For synchronous counter $f_{max} = \frac{1}{x} = \frac{1}{5\,\mu S} = 0.2$ MHz = 200 KHz

When multiple counters are connected in cascade, then the total number of states of the new counter is $A \times B \times C$. That is, it will work as mod $-A \times B \times C$ counter.



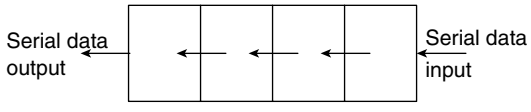
For example, decade counter counts from 0 to 9, 10 states—If two such decade counters are connected in cascade, then the total counting states will be $10 \times 10 = 100$, it will work as mod -100 counter, which counts from 00 to 99.

Registers

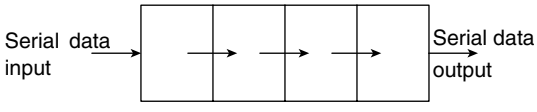
A number of flip-flops connected together such that data may be shifted into and shifted out of them is called a shift register. There are four basic types of shift register.

(1) Serial-in serial-out
(2) Serial-in parallel-out
(3) Parallel-in parallel-out
(4) Parallel-in serial-out

Serial in Serial out

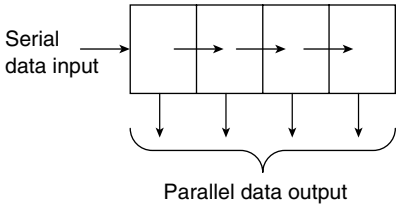


Serial–in, serial-out, shift-left, shift register

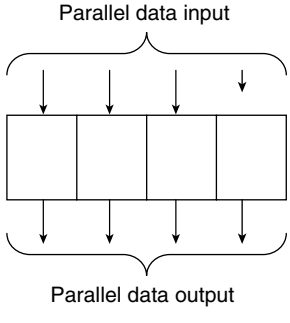


Serial–in, serial-out, shift-right, shift register

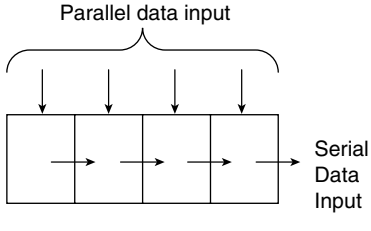
Serial in Parallel out



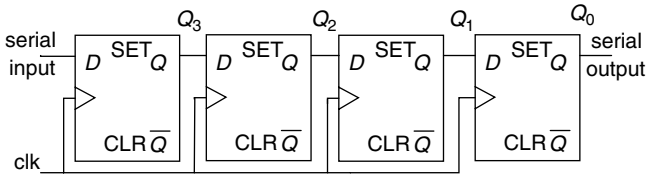
Parallel in – Parallel out



Parallel in, Serial Out



Serial input and serial output register: This type of shift register accepts data serially, that is, one bit at a time and also outputs data serially. The logic diagram of 4-bit serial input, serial output, shift right, shift register is shown in figure. With four D flip-flops the register can store up to four bits of data.



If initially all flip-flops are reset, then by applying serial input 1101, the flip-flop states will change as shown in below table.

Clk	S.I	Q_3	Q_2	Q_1	Q_0
0	1	0	0	0	0
1	0	1	0	0	0
2	1	0	1	0	0
3	1	1	0	1	0
4		1	1	0	1

The first data bit 1 will appear at serial output after 4 clock pulses.

Application of Shift Registers

1. Delay line: Serial input and serial output shift register can be used to introduce delay in digital signals.

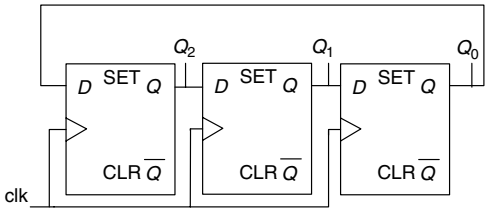
$$\text{delay} = \text{no.of flip-flops} \times \frac{1}{\text{clk frequency}}$$

$$= \text{no. of flip-flops} \times \text{Time period of clock pulse}$$

2. Serial to parallel, parallel to serial converter: SIPO, PISO registers used for data conversion.
3. Sequence generator: A circuit which generates a prescribed sequence of bits, with clock pulses is called as sequence generator
   The minimum number of flip-flops 'n' required to generate a sequence of length 'S' bits is given by $S \leq 2^n - 1$

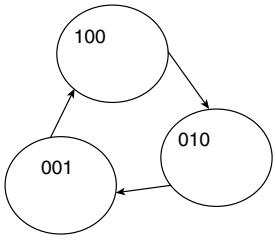
Shift Register Counters

One of the applications of the shift register is that they can be arranged to form as ring counters. Ring counters are constructed by modifying the serial in, serial out, shift registers. There are two types of ring counters—basic ring counter, twisted ring counter (Johnson counter). The basic ring counter is obtained from SISO shift register by connecting serial output to serial input.



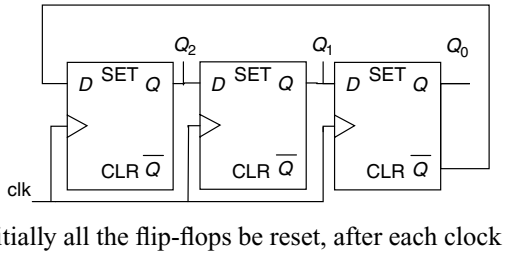
In most instances only a single 1 or single 0 is in the register and is made to circulate around the register as long as the clock pulses are applied. Consider initially first flip-flop is set, and others are reset. After three clock pulses again, we will get initial state of 100. So this is a mod-3 counter.

clk	Q_2	Q_1	Q_0
0	1	0	0
1	0	1	0
2	0	0	1
3	1	0	0
4	0	1	0



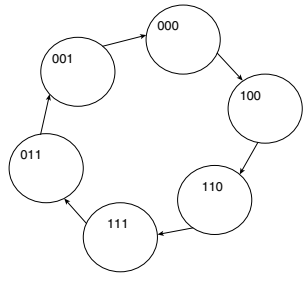
A ring counter with N flip-flops can count up to N states, that is, mod –N counter, whereas N-bit asynchronous counter can count up to 2^N states. So ring counter is uneconomical compared to a ripple counter but has the advantage of requiring no decoder. Since it is entirely synchronous operation and requires no gates for flip-flop inputs, it has further advantage of being very fast.

Twisted ring counter (Johnson counter): This counter is obtained from a SISO shift register by connecting the complement of serial output to serial input as shown in below figure.



Let initially all the flip-flops be reset, after each clock pulse the complement of last bit will appear as at MSB, and other bits shift right side by one bit. After six clock pulses, the register will come to initial state 000. Similarly, the 3-bit Johnson counter will oscillate between the states 101, 010.

clk	Q_2	Q_1	Q_0
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0



An n-bit Johnson counter can have $2n$ unique states and can count up to $2n$ pulses, so it is a mod-$2n$ counter. It is more economical than basic ring counter but less economical than ripple counter.

Example 9

Assume that 4-bit counter is holding the count 0101. What will be the count after 27 clock pulses?

Solution

Total clock pulses: $27 = 16 + 11$

$$0101 + 1011 = 0000$$

Example 10

A mod – 2 counter followed by mod – 5 counter is

Solution

A decade counter, counts 10 states (5×2)

Example 11

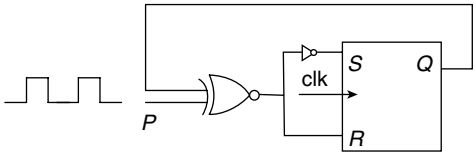
A 4-bit binary ripple counter uses flip-flops with propagation delay time of 25 ms each. The maximum possible time required for change of state will be

Solution

The maximum time = 4×25 m.s = 100 m.s

Example 12

Consider the circuit, the next state Q^+ is



Solution

P	Q	S	R	Q^+
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0

So, $Q^+ = P \oplus Q$

Example 13

A certain J-K *FF* has $t_{pd} = 12$ ns. What is the largest MOD counter that can be constructed from these *FF* and still operate up to 10 MHz

Solution

$$N \le \frac{1}{f_{max} . t_{pd}}$$

$F_{max} = 10$ MHz $N \le 8$

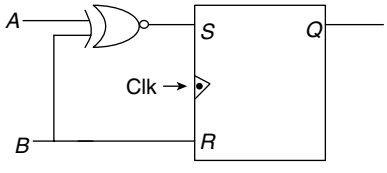
$t_{pd} = 12$ n seconds

$$N \le \frac{1}{10\times10^6 \times12\times10^{-9}}$$

Mod counter is $= 2^N = 2^8 = 256$

Example 14

An AB flip-flop is constructed from an S-R flip-flop as shown below. The expression for next state Q^+ is



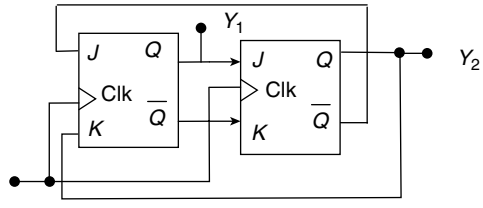
Solution

A	B	Q	S	R	Q^+
0	0	0	1	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	1	×
1	1	1	1	1	×

$\therefore Q^+ = \overline{A}\overline{B} + AQ = \overline{A}\overline{B} + \overline{B}Q$

Example 15

In the circuit shown below, the output y_1 and y_2 for the given initial condition $y_1 = y_2 = 1$ and after four input pulses will be



Solution

After 1st pulse, $y_1 = 0\ y_2 = 1$
After 2nd pulse, $y_1 = 0\ y_2 = 0$
After 3rd pulse, $y_1 = 1\ y_2 = 0$
After 4th pulse, $y_1 = 1\ y_2 = 1$

Example 16

A ripple counter is to operate at a frequency of 10 MHz. If the propagation delay time of each flip-flop in the counter is 10 ns and the storing time is 50 ns, how many maximum stages can the counter have?

Solution

$$nt_{pd} + t_s \le \frac{1}{f}$$

Where n = number of stages

T_{pd} = propagation delay time

T_s = strobing time

F = frequency of operation $= 10 \times 10^{-9}n + 50 \times 10^{-9}$

$$\le \frac{1}{10\times10^6}$$

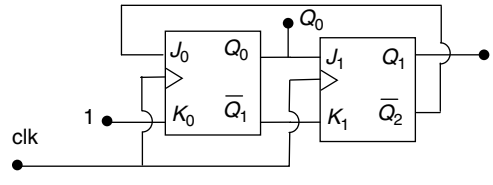
(or) $10n + 50 \le 100$

(or) $10n \le 50$

For max stages n $\frac{50}{10} = 5$

Example 17

In the circuit assuming initially $Q_0 = Q_1 = 0$. Then the states of Q_0 and Q_1 immediately after the 33rd pulse are



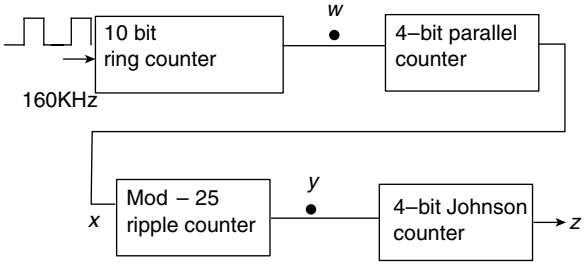
Solution

J_0	K_0	J_1	K_1	Q_0	Q_1	Count
1	1	0	1	0	0	Initial
1	1	1	0	1	0	1st pulse
0	1	0	1	0	1	2nd
1	1	0	1	0	0	3rd
1	1	1	0	1	0	4th
0	1	0	1	0	1	5th pulse

After 4th pulse, output is same as after 1st one. So, the sequence gets repeated. So output after 33rd pulse would be same as after 3rd pulse, that is, (00)

Example 18

The frequency of the pulse at z in the network shown in figure is

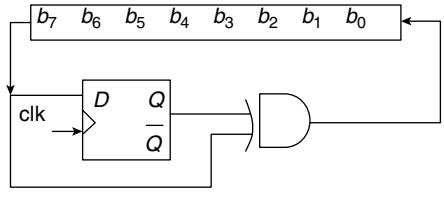


Solution

10-bit ring counter is a Mod – 10. So, it divides the 160 KHz input by 10. Therefore, w = 16 KHz. The four-bit parallel counter is a Mod – 16. Thus, the frequency at x = 1 KHz. The mod – 25 ripple counter produces a frequency at y = 40 Hz (1 KHz/25 = 40 Hz). The four-bit Johnson counter is a Mod – 8. The frequency at Z = 5 Hz

Example 19

The 8-bit shift left shift register, and D flip-flop shown in the figure is synchronized with the same clock. The D flip-flop is initially cleared. The circuit acts as follows:



Solution

The output of XOR gate is $Z = b_{i+1} \oplus b_i$ and this output shift the register to left, Initially $Z = 0$

After 2nd clock $Z = b_7 \oplus 0 = b_7$
After 2nd clock $Z = b_7 \oplus b_6$
3rd clock $Z = b_6 \oplus b_5$
4th clock $Z = b_5 \oplus b_4$
It is a binary to grey code converter.

Example 20

A 4-bit mod – 16 ripple counter uses J-K flip-flops. If the propagation delay of each flip-flop is 50 ns, the maximum clock frequency that can be used is equal to

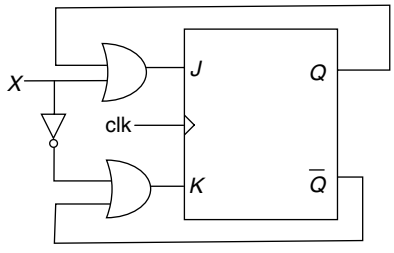
Solution

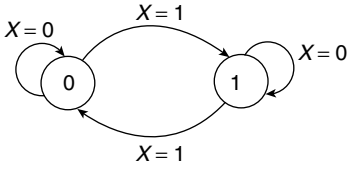
$$\text{max} = \text{clock frequency} = \frac{1}{4 \times 50 \times 10^{-9}}$$

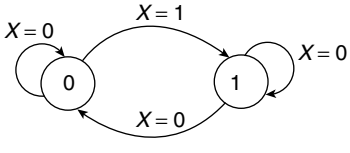
$$= 5 \text{ MHz}$$

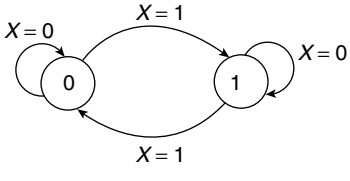
Example 21

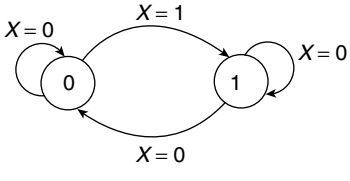
What is the state diagram for the sequential circuit shown?



(A) 

(B) 

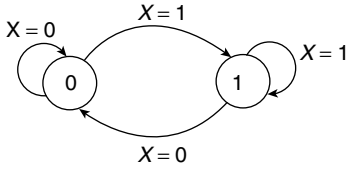
(C) 

(D) 

Solution

State diagram of a sequential circuit will have states (output) of all the flip-flops

Present state	Next state Q_{n+1}	
Q_n	For $x = 0$	For $x = 1$
0	0	1
1	0	1



Hence, the correct option is (D).

EXERCISES

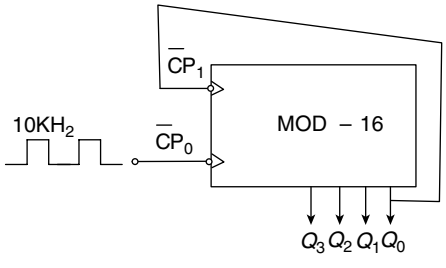
Practice Problems I

Direction for questions 1 to 25: Select the correct alternative from the given choices.

1. How many flip-flops are needed for MOD – 16 ring counter and MOD – 16 Johnson counter
(A) 16, 16 (B) 16, 8 (C) 4, 3 (D) 4, 4

2. A 2 - bit synchronous counter uses flip-flops with propagation delay time of 25 ns, each. The maximum possible time required for change of state will be
(A) 25 ns (B) 50 ns (C) 75 ns (D) 100 ns

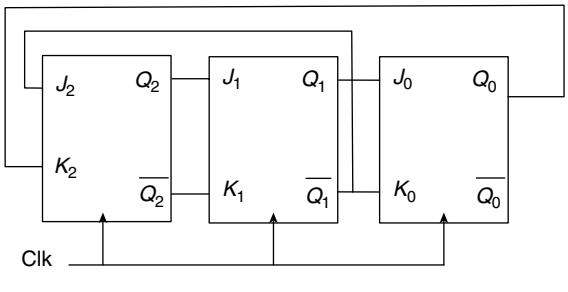
3. For given MOD – 16 counter with a 10 KHz clock input determine the frequency at Q_3



(A) 625 Hz (B) 10 kHz (C) 2.5 kHz (D) 0 Hz

4. A 4-bit ripple counter and a 4-bit synchronous counter are made using flip-flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S, respectively. then
(A) $R = 10$ ns, $S = 40$ ns
(B) $R = 40$ ns, $S = 10$ ns
(C) $R = 10$ ns, $S = 30$ ns
(D) $R = 30$ ns, $S = 10$ ns

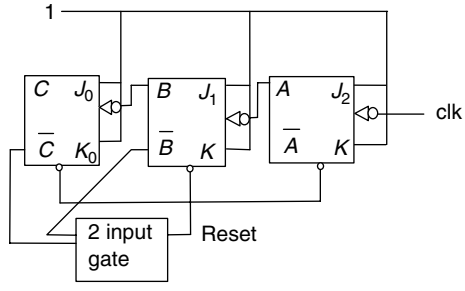
5. The counter shown in the figure has initially $Q_2Q_1Q_0 =$ 000. The status of $Q_2Q_1Q_0$ after the first pulse is



(A) 001 (B) 010 (C) 100 (D) 101

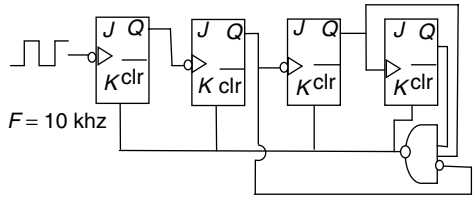
6. 12 MHz clock frequency is applied to a cascaded counter of MOD – 3 counter, MOD – 4 counter and MOD – 5 connecter. The lowest output frequency is?
(A) 200 kHz (B) 1 MHz
(C) 3 MHz (D) 4 MHz

7. In the modulo – 6 ripple counter shown in figure below, the output of the 2 – input gate is used to clear the J-K flip-flops. The two input gate is



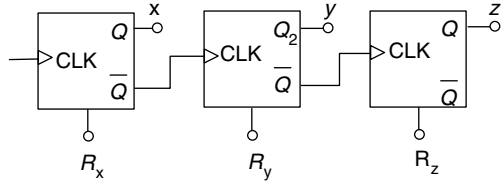
(A) a NAND gate (B) a NOR gate
(C) an OR gate (D) an AND gate

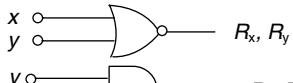
8. In figure, J and K inputs of all the four flip-flops are made high, the frequency of the signal at output y is

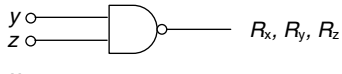


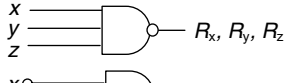
(A) 0.833 kHz (B) 1.0 kHz
(C) 0.91 kHz (D) 0.77 kHz

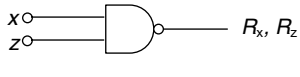
9. In a number system, a counter has to recycle to 0 at the sixth count. Which of the connections indicated below will realize this resetting? (a logic '0' at the R inputs resets the counters)



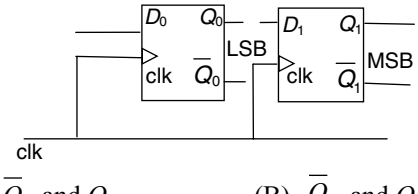
(A) 

(B) 

(C) 

(D) 

10. Two D flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following Q_1Q_0 sequence 00 → 01 → 11 → 10 → 00. The inputs D_0 and D_1 respectively should beconnected as

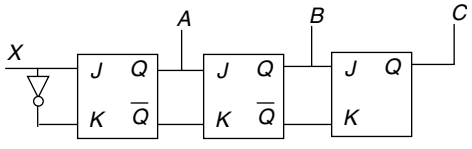


(A) $\overline{Q}_1$ and Q_0 (B) $\overline{Q}_0$ and Q_1
(C) $\overline{Q}_1\overline{Q}_0$ and $\overline{Q}_1Q_0$ (D) $\overline{Q}_1\overline{Q}_0$ and $\overline{Q}_1Q_0$

11. N flip-flops can be used to divide the input clock frequency by

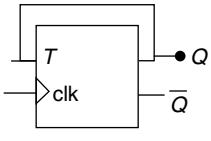
(A) N (B) $2N$ (C) 2^N (D) 2^{N-1}

12. For a shift register as shown, $x = 1011$, with initially FF cleared, ABC will have value of – after three clock pulses



(A) 101 (B) 011 (C) 001 (D) 111

13. If a FF is connected as shown what will be the output? (initially $Q = 0$)



(A) 11111 (B) 0000 (C) 1010 (D) 0101

14. The excitation table for a flip-flop whose output conditions are,

if $AB = 00$, no change of state occurs,

$AB = 01$, ff becomes 1 with next clock pulse,

$AB = 10$, ff becomes 0 with next clock pulse,

$AB = 11$, ff changes its state

(A)

Q_n	Q_{n+1}	A	B
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(B)

Q_n	Q_{n+1}	A	B
0	0	1	x
0	1	0	x
1	0	x	0
1	1	x	1

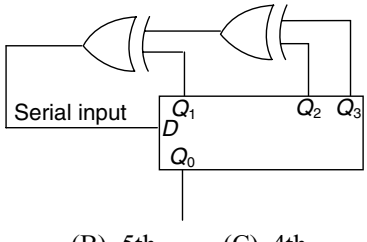
(C)

Q_n	Q_{n+1}	A	B
0	0	x	0
0	1	x	1
1	0	x	x
1	1	0	x

(D)

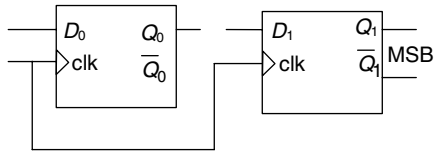
Q_n	Q_{n+1}	A	B
0	0	x	0
0	1	1	x
1	0	x	1
1	1	0	x

15. A shift register that shift the bits 1 position to the right at each clock pulse is initialized to 1100 (Q_0, Q_1, Q_2, Q_3). The outputs are combined using an XOR gate circuit and fed to the D input. After which clock pulse will the initial pattern reappear at the output?



(A) 6th (B) 5th (C) 4th (D) 7th

16. If we need to design a synchronous counter that goes through the states $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$ using D flip-flop, what should be the input to the flip-flops?



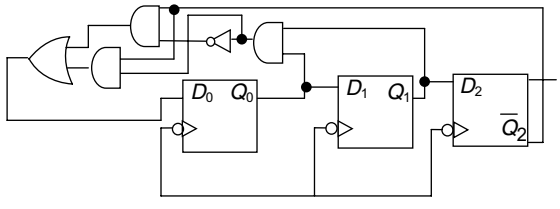
(A) $D_0 = Q_0, D_1 = \overline{Q_1}$

(B) $D_0 = \overline{Q_1}, D_1 = Q_0$

(C) $D_0 = \overline{Q_1}.Q_0, D_1 = \overline{Q_1}\ \overline{Q_0}$

(D) $D_0 = \overline{Q_0}, D_1 = Q_1$

17. Find the counter state sequence (Assume Q_0 as MSB).



(A) 4, 6, 7, 3, 1, 0, 4 (B) 4, 6, 5, 3, 1, 0, 4

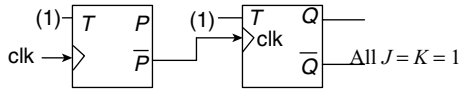
(C) 4, 5, 6, 7, 0, 4, 5 (D) 4, 6, 7, 1, 0, 4

18. If the propagation delay of each flip-flop is 50 ns, and for the AND gate to be 20 ns. What will be the f_{max} for mod 32 ripple and synchronous counters?

(A) 14.3 MHz, 4 MHz (B) 14.3 MHz, 5 MHz

(C) 5 MHz, 14.3 MHz (D) 3.7 MHz, 14.3 MHz

19. For a given counter identify its behaviour

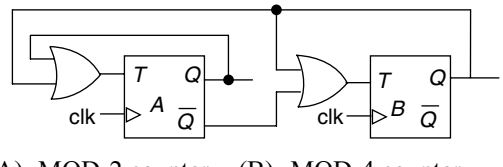


The output is taken from PQ.

(A) mod-4 up counter (B) mod-2 down counter

(C) mod-4 down counter (D) mod-2 up counter

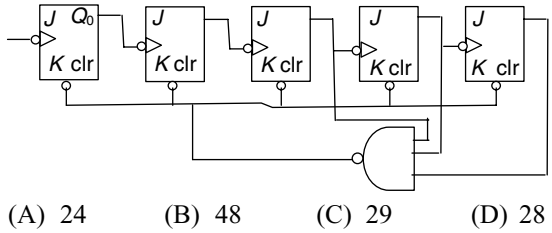
20. A circuit using T flip-flop is given. Identify the circuit.



(A) MOD-2 counter (B) MOD-4 counter

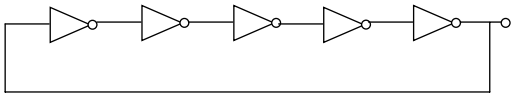
(C) MOD-3 counter (D) MOD-2 generate 00, 10, 00

21. The mod number of asynchronous counter shown



(A) 24 (B) 48 (C) 29 (D) 28

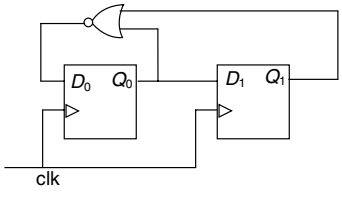
22. For the oscillator find the fundamental frequency if propagation delay of each inverter is 1,000 psec.



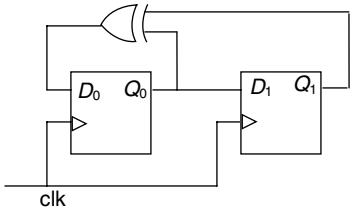
(A) 100 MHz (B) 10 MHz (C) 1 GHz (D) 10 GHz

23. Which of the following represent mod-3 synchronous up counter?

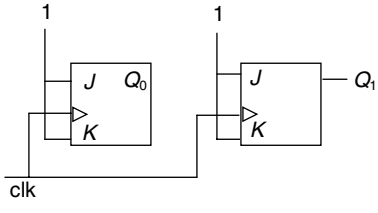
(P)



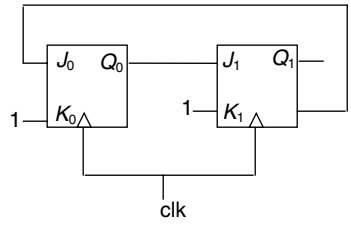
(Q)



(R)

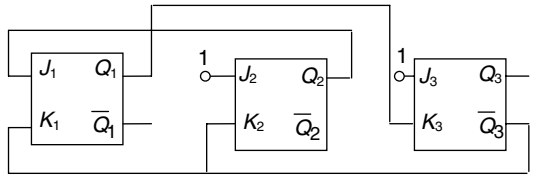


(S)



(A) P, Q, R, S (B) P, S
(C) P, Q, S (D) P, Q

24. Identify the output sequence (Assume all outputs to be 1 initially), of Synchronous counter?



(A) 7, 3, 4, 6, 7 (B) 2, 4, 6, 7, 2
(C) 7, 4, 7, 3 (D) 7, 6, 7, 3

25. If by using a modulo 1,024 ripple counter we need to count a pulse train having a frequency of 1 MHz, what is the maximum permissible propagation delay of each flip-flop?

(A) 100 ns (B) 50 ns
(C) 20 ns (D) 10 ns

Practice Problems 2

Direction for questions 1 to 30: Select the correct alternative from the given choices.

1. Match List-I (operation) with List-II (associated device) and select the correct answer using the codes given below:

List-I	List-II
(a) Frequency division	(1) ROM
(b) Decoding	(2) Multiplexer
(c) Data selection	(3) De multiplexer
(d) Code conversion	(4) Counter

(A) a – 3, b – 4, c – 2, d – 1 (B) a – 3, b – 4, c – 1, d – 2
(C) a – 4, b – 3, c – 1, d – 2 (D) a – 4, b – 3, c – 2, d – 1

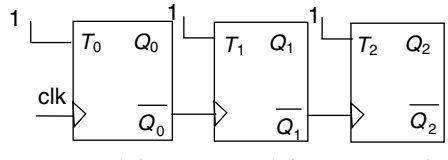
2. A mod – 5 synchronous counter is designed by using J-K flip-flops, the number of counts skipped by it, will be

(A) 2 (B) 3 (C) 5 (D) 0

3. A counter starts off in the '0000' state, then clock pulses are applied. Sometimes later the clock pulses are removed and the counter flip-flops read '0011'. How many clock pulses have occurred?

(A) 3 (B) 35
(C) 51 (D) any of these

4. Figure below shown as ripple counter using positive edge triggered flip-flops. If the present state of the counters is $Q_2\,Q_1\,Q_0 = 011$, then its next state ($Q_2Q_1Q_0$) will be

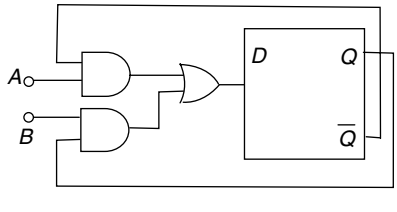


(A) 010 (B) 100 (C) 111 (D) 101

5. A synchronous sequential circuit is designed to detect a bit sequence 0101 (overlapping sequence include). Every time this sequence is detected, the circuit produces output of '1'. What is the minimum number of states the circuit must have?

(A) 4 (B) 5 (C) 6 (D) 7

6. What is represented by digital circuit given below?



(A) An S–R flip-flop with $A = S$ and $B = R$
(B) A J-K flip-flop with $A = K$ and $B = J$
(C) A J-K flip-flop with $A = J$ and $B = \overline{K}$
(D) An S-R flip-flop with $A = R$ and $B = S$

7. In a ripple counter the state whose output has a frequency equal to $\frac{1}{8}th$ that of clock signal applied to the first stage, also has an output periodically equal to $\frac{1}{8}th$ that of the output signal obtained form the last stage. The counter is
(A) mod – 8 (B) mod – 6
(C) mod – 64 (D) mod – 16

8. A flip-flop is popularly known as
(A) a stable multivibrator
(B) bistable multivibrator
(C) monostable multivibrator
(D) none of these

9. Which of the following represents the truth table for J-K flip-flop?

(A)

J	K	output
0	0	Q_0
0	1	0
1	0	1
1	1	$\overline{Q_0}$

(B)

J	K	output
0	0	$\overline{Q_0}$
0	1	0
1	0	1
1	1	Q_0

(C)

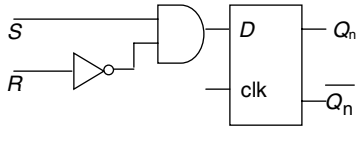
J	K	output
0	0	Q_0
0	1	0
1	0	1
1	1	invalid

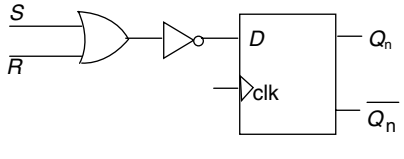
(D)

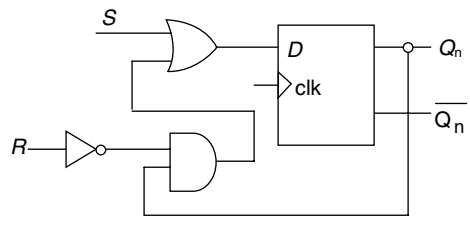
J	K	output
0	0	1
0	1	0
1	0	1
1	1	0

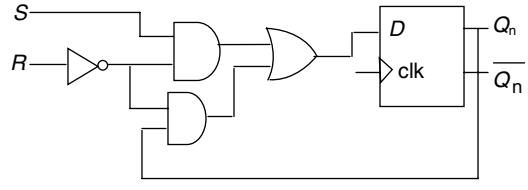
10. One disadvantage of master-slave flip-flop is
(A) setup time becomes longer
(B) it requires input to be held constant before clock transition
(C) unpredictable output even if input held constant
(D) hold time becomes longer

11. Which of the following converts D flip-flop to S-R flip-flop?

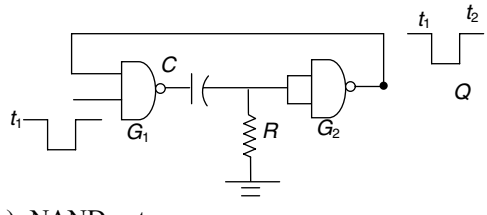
(A)


(B)


(C)


(D)


12. Which of the circuit is being represented by the figure?



(A) NAND gate
(B) Monostable multivibrator
(C) Astable multivibrator
(D) Schmitt trigger

13. Hold time is
(A) time for which output is held constant
(B) time for which clock is to be held constant on applying input
(C) time for which input should be maintained constant after the triggering edge of clock pulse
(D) time for which input should be maintained constant prior to the arrival of triggering edge of clock pulse

14. Shift registers are made up of
(A) MOS inverters (B) *FF*
(C) latches (D) none of these

15. Data from a satellite is received in serial form. If the data is coming at 8 MHz rate, how long will it take to serially load a word in 40 bit shift register?
(A) 1.6 μs (B) 5 μs
(B) 6.4 μs (D) 12.8 μs

16. A J-K flip-flop can be converted into T flip-flop by connecting
(A) $\overline{Q}$ to 0
(B) 0 to $\overline{Q}$
(C) 0 to Q
(D) by connecting both J and K inputs to T

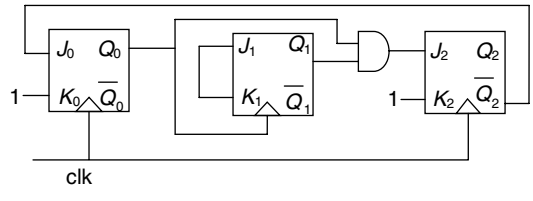
17. The flip-flop that is not affected by race around condition
(A) T flip-flop (B) J-K flip-flop
(C) S-R flip-flop (D) None of these

18. The characteristic equation of J-K flip-flop is
(A) $J'Q(t) + KQ'(t)$ (B) $J'Q(t) + KQ(t)$
(C) $JQ'(t) + K'Q(t)$ (D) None of these

19. For a D flip-flop input, the $S\ \overline{Q}$ is connected. What would be the output sequence?
(A) 0000 (B) 1111
(C) 010101 (D) 101010

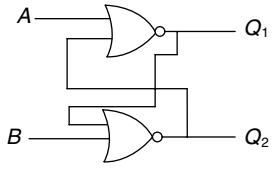
20. In order to implement a mod 6 synchronous counter we have 3 *FF* and a combination of 2 input gate(s). Identify the combination circuit?
(A) one AND gate
(B) one OR gate
(C) one AND and one OR gate
(D) two AND gates

21. Given a MOD-5 counter. The valid states for the counter are (0, 1, 2, 3, 4). The propagation delay of each *ff* is T_F and that of AND gate is t_A. The maximum rate at which counter will operate satisfactorily



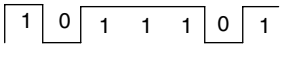
(A) $\dfrac{1}{t_F + t_A}$ (B) $\dfrac{1}{3t_F}$
(C) $\dfrac{1}{2t_F + t_A}$ (D) $\dfrac{1}{3t_F - t_A}$

22. For a NOR latch as shown up A and B are made first (0, 1) and after a few seconds it is made (1, 1). The corresponding output (Q_1, Q_2) are



(A) first (1, 0) then (0, 0) (B) first (1, 0) then (1, 0)
(C) first (1, 0) then (1, 1) (D) first (1, 0) then (0, 1)

23. In order to design a pulse generator to generate the wave form using a shift register, what is the no. of *FF* required?

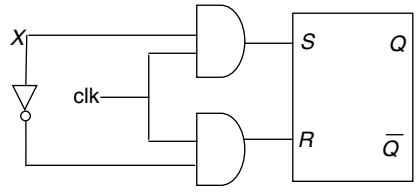


(A) 3 (B) 4 (C) 5 (D) 6

24. For what minimum value of propagation delay in each *FF* will a 10-bit ripple counter skip a count when it is clocked at 5 MHz?
(A) 10 ns (B) 20 ns (C) 25 ns (D) 15 ns

25. A divide by 50 counter can be realized by using
(A) 5 no. of mod-10 counter
(B) 10 no. of mod-5 counter
(C) one mod-5 counter followed by one mod-10 counter
(D) 10 no. of mod-10 counter

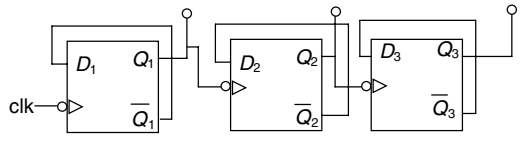
26. The following latch is



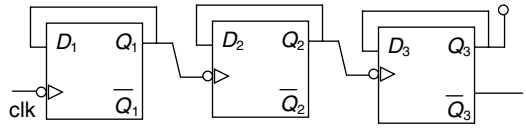
(A) D latch (B) T latch
(C) J-K latch (D) R-S latch

27. Which of the following represent a 3 bit ripple counter using D flip-flops?

(A)

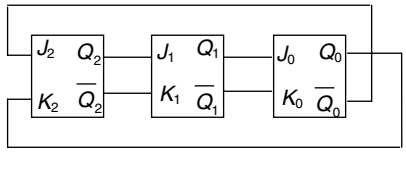


(B)



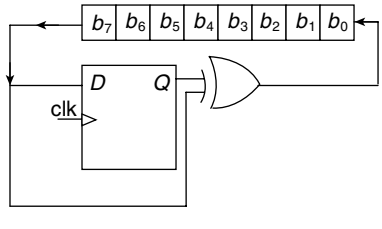
(C) both (A) and (B)
(D) none of these

28. For the Johnson counter with initial Q_2, Q_1, Q_0 as 101, the frequency of the output is (Q_2, Q_1, Q_0)



(A) $\dfrac{f_C}{8}$ (B) $\dfrac{f_C}{6}$ (C) $\dfrac{f_C}{2}$ (D) $\dfrac{f_C}{4}$

29. For the given circuit the contents of register ($b_7 - b_0$) are 10010101, what will be the register contents after 8 clock pulses?



(A) 10010101 (B) 01101010
(C) 11011111 (D) 01101011

30. A latch is to be build with *A* and *B* as input. From the table find the expression for the next state Q^+

A	B	Q	Q^+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(A) A (B) B
(C) $A + \overline{B}$ (D) $A\overline{B} + AB$

Previous Years' Questions

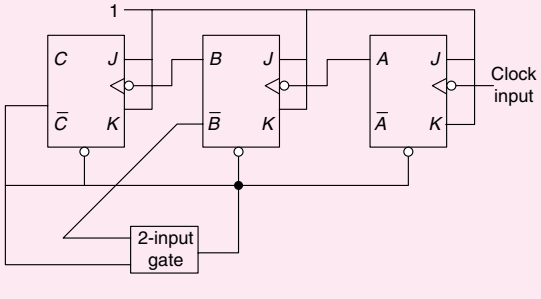
1. A master slave flip -flop has the characteristic that **[2004]**
(A) Change in the input immediately reflected in the output
(B) Change in the output occurs when the state of the master is affected
(C) Change in the output occurs when the state of the salve is affected
(D) Both the master rand the slave states are affected at the same time

2. Choose the correct one from among the alternatives A, B, C and D after matching an item from Group 1 with the most appropriate item in Group 2. **[2004]**

Group 1		Group 2	
P	Shift register	1	Frequency division
Q	Counter	2	Addressing in memory chips
R	Decoder	3	Serial to parallel data conversion

(A) $P-3,\ Q-2,\ R-1.$ (B) $P-3,\ Q-1,\ R-2.$
(C) $P-2,\ Q-1,\ R-3.$ (D) $P-1,\ Q-2,\ R-2.$

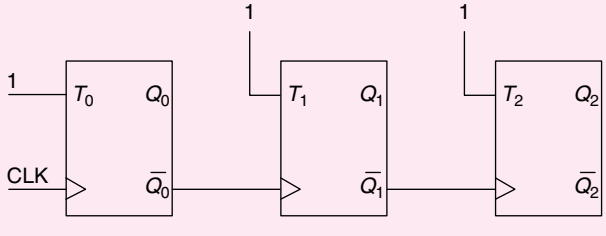
3. In the modulo -6 ripple counter shown in figure, the output of the 2 -input gate is used to clear the J-K flip-flops. **[2004]**



The 2 -input gate is :
(A) a NAND gate
(B) a NOR gate
(C) an OR gate
(D) an AND gate

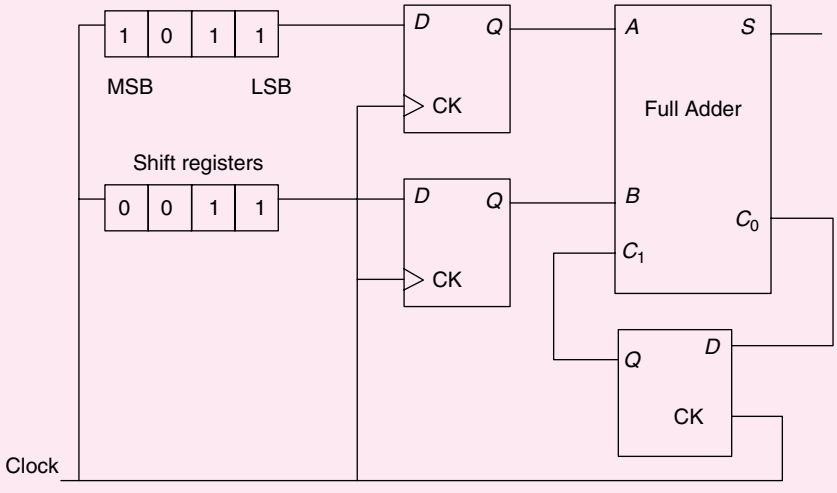
4. The present output Q of an edge triggered J-K flip-flop is logic 0. If $J = 1$, then Q_{n+1} **[2005]**
(A) cannot be determined
(B) will be logic 0
(C) will be logic 1
(D) will race around

5. Figure shows a ripple counter using positive edge triggered flip-flops. If the present state of counter is $Q_2Q_1Q_0 = 011$, then its next state $(Q_2Q_1Q_0)$ will be **[2005]**



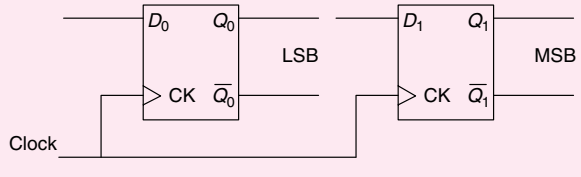
(A) 010 (B) 100
(C) 111 (D) 101

6. For the circuit shown in figure below, two 4-bit parallel in serial out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in clear state. After applying two clock pulses, the outputs, of the full-adder should be **[2006]**



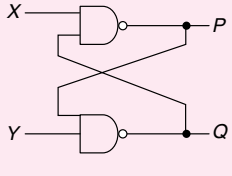
(A) $S = 0, C_0 = 0$
(B) $S = 0, C_0 = 1$
(C) $S = 1, C_0 = 0$
(D) $S = 1, C_0 = 1$

7. Two D flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following Q_1Q_0 sequence
$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow$ .....
The inputs D_0 and D_1, respectively should be connected as **[2006]**



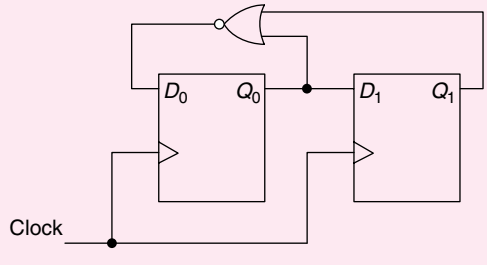
(A) $\overline{Q_1}$ and Q_0
(B) $\overline{Q}_0$ and Q_1
(C) $\overline{Q}_1Q_0$ and $\overline{Q}_1Q_0$
(D) $\overline{Q}_1$ $\overline{Q}_0$ and Q_1Q_0

8. The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:
$X = 0, Y = 1, X = 0, Y = 0; X = 1\ Y = 1$
The corresponding stable P, Q outputs will be:
[2007]



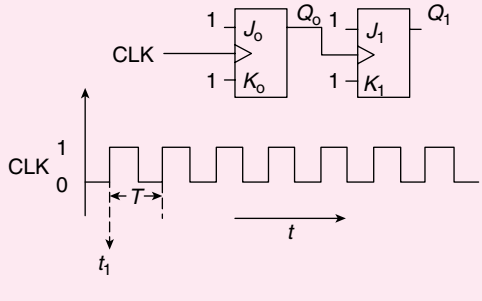
(A) $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$
(B) $P = 1, Q = 0; P = 0, Q = 1;$ or $P = 0, Q = 1, P = 0, Q = 1$
(C) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0$ or $P = 0, Q = 1$
(D) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1$

9. For the circuit shown the counter state (Q_1 Q_0) follows the sequence **[2007]**

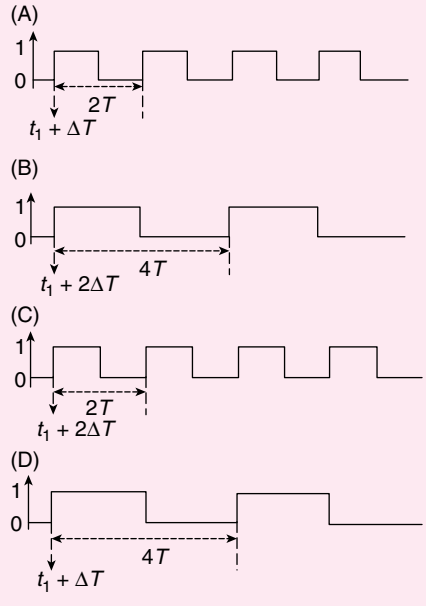


(A) 00, 01, 10, 11, 00…….
(B) 00, 01, 10, 00, 01…….
(C) 00, 01, 11, 00, 01……
(D) 00, 10, 11, 00, 10…….

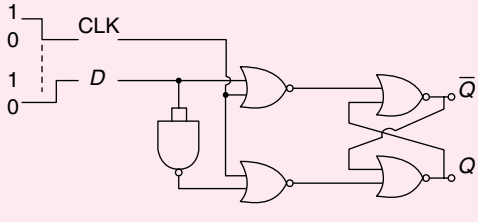
10. For each of the positive edge-triggered J-K flip-flop used in the following figure, the propagation delay is ΔT **[2008]**



Which of the following waveforms correctly represents the output at Q_1?



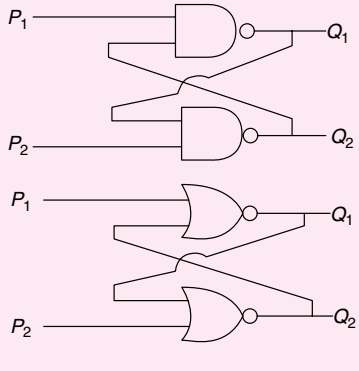
11. For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible **[2008]**



Which of the following statements is true?

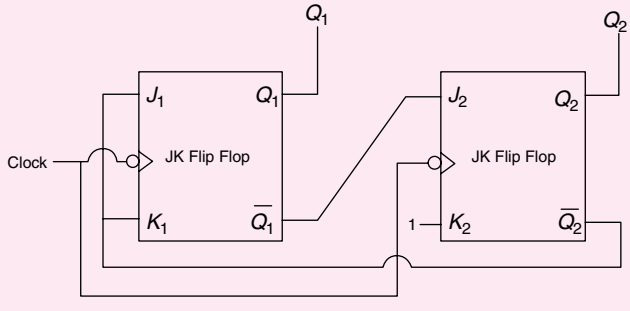
(A) Q goes to 1 at the CLK transition and stays at 1
(B) Q goes to 0 at the CLK transition and stays at 0
(C) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1
(D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

12. Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are **[2009]**



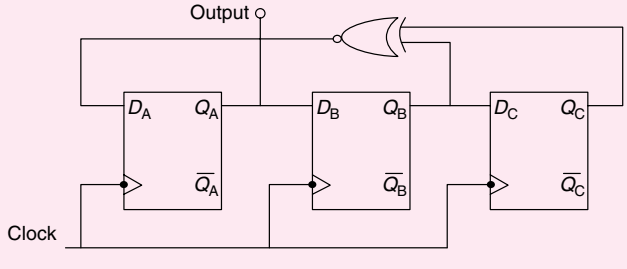
(A) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
(B) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (1, 0)
(C) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)
(D) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)

13. What are the counting stages (Q_1, Q_2) for the counter shown in the figure below? **[2009]**



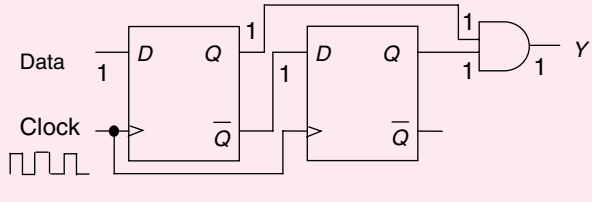
(A) 11, 10, 00, 11, 10,.... (B) 01, 10, 11, 00, 01,....
(C) 00, 11, 01, 10, 00,.... (D) 01, 10, 00, 01, 10,....

14. Assuming that flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is **[2010]**



(A) 0010111… (B) 0001011…
(C) 0101111… (D) 0110100…

15. When the output Y in the circuit below is '1', it implies that data have **[2011]**



(A) changed from '0' to '1'
(B) changed from '1' to '0'
(C) changed in either direction
(D) not changed

16. Two D flip-flops are connected as a synchronous counter that goes through the following Q_B Q_A sequence $00 \rightarrow 11 \rightarrow 01 \rightarrow 00 \rightarrow \ldots$

The connections to the inputs D_A and D_B are **[2011]**

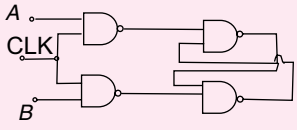
(A) $D_A = Q_B, D_B = Q_A$

(B) $D_A = \overline{Q}_A, D_B = \overline{Q}_B$

(C) $D_A = (Q_A \overline{Q}_B + \overline{Q}_A Q_B), D_B = Q_A$

(D) $D_A = (Q_A Q_B + \overline{Q}_A \overline{Q}_B), D_B = \overline{Q}_B$

17. Consider the given circuit



In this circuit, the race around **[2012]**

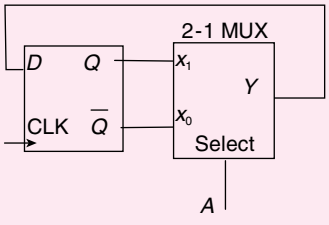
(A) Does not occur

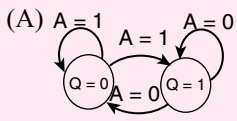
(B) Occurs when CLK = 0

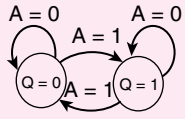
(C) Occurs when CLK = 1 and $A = B = 1$

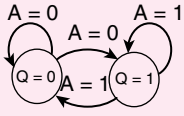
(D) Occurs when CLK = 1 and $A = B = 0$

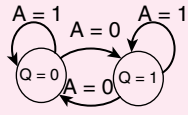
18. The state transition diagram for the logic circuit shown is **[2012]**



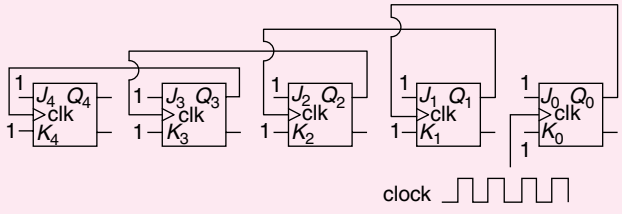
(A) 

(B) 

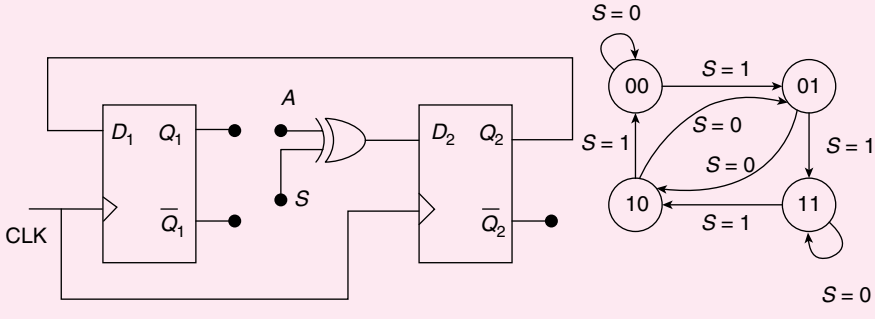
(C) 

(D) 

19. Five J-K flip-flops are cascaded to form the circuit shown in Figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q_3 is _____. **[2014]**



20. The digital logic shown in the figure satisfies the given state diagram when Q_1 is connected to input A of the XOR gate.



Suppose the XOR gate is replaced by an XNOR gate. Which one of the following options preserves the state diagram? **[2014]**

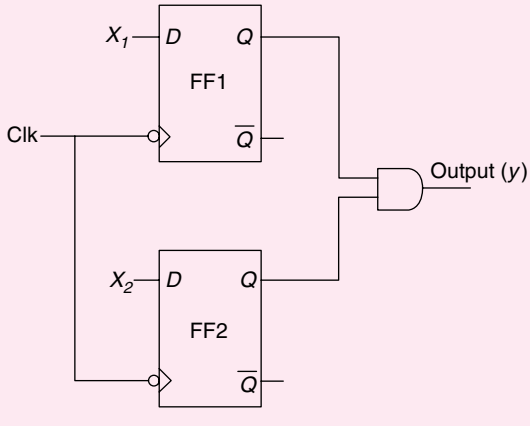
(A) Input A is connected to $\overline{Q}_2$

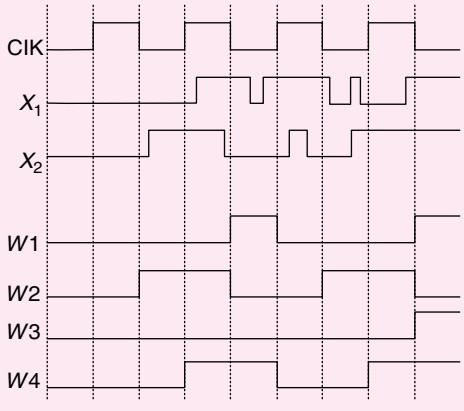
(B) Input A is connected to Q_2

(C) Input A is connected to $\overline{Q}_1$ and S is complemented

(D) Input A is connected to $\overline{Q}_1$

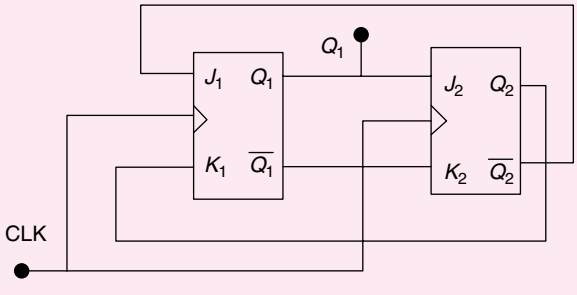
21. In the circuit shown, choose the correct timing diagram of the output (y) from the given waveforms $W1$, $W2$, $W3$, and $W4$. **[2014]**





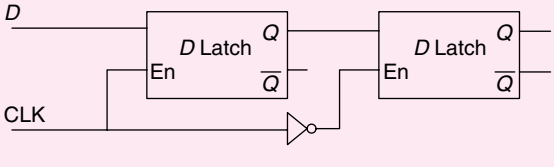
(A) $W1$ (B) $W2$
(C) $W3$ (D) $W4$.

22. The outputs of the two flip-flops Q_1, Q_2 in the figure shown are initialized to 0, 0. The sequence generated at Q_1 upon application of clock signal is **[2014]**



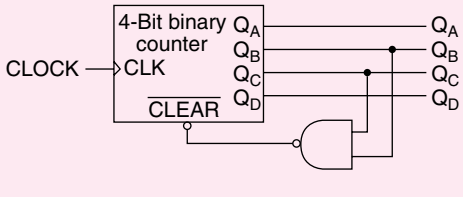
(A) 01110… (B) 01010….
(C) 00110… (D) 01100….

23. The circuit shown in the figure is a **[2014]**

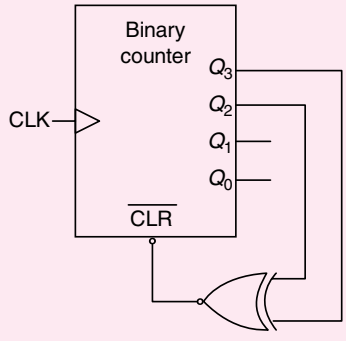


(A) Toggle Flip-Flop
(B) J-K Flip-Flop
(C) S-R Latch
(D) Master-Slave D Flip-Flop

24. A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. The value of n is _____. **[2015]**



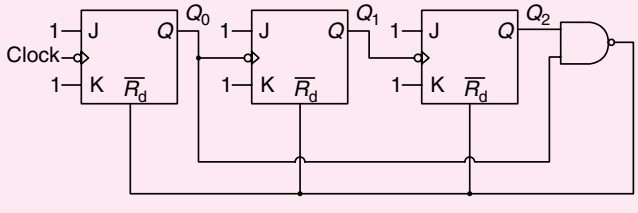
25. The figure shows a binary counter with synchronous clear input. With the decoding logic shown, the counter works as a **[2015]**



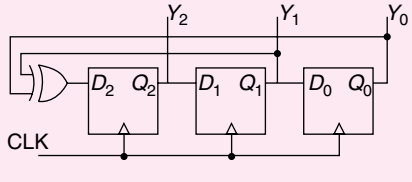
(A) mod-2 counter (B) mod-4 counter
(C) mod-5 counter (D) mod-6 counter

26. The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset $\left(\overline{R_d} \text{ input}\right)$. The counter corresponding to this circuit is **[2015]**

(A) a modulo-5 binary up counter
(B) a modulo-6 binary down counter
(C) a modulo-5 binary down counter
(D) a modulo-6 binary up counter

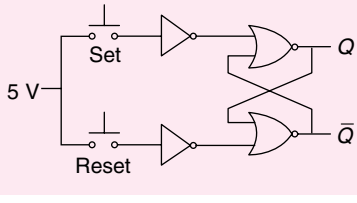


27. A three-bit pseudorandom number generator is shown. Initially, the value of output $Y = Y_2\ Y_1\ Y_0$ is set to 111. The value of output Y after three clock cycles is **[2015]**



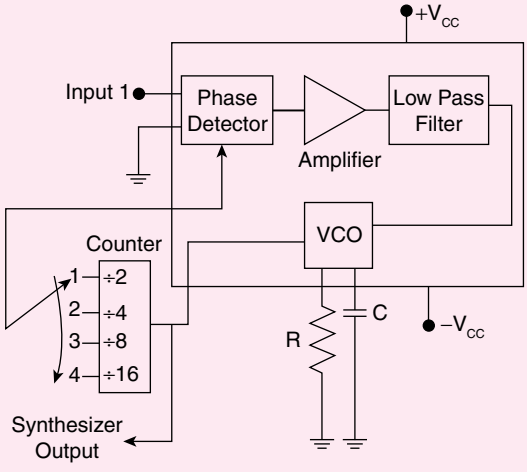
(A) 000 (B) 001
(C) 010 (D) 100

28. An SR latch is implemented using TTL gates as shown in the figure. The set and reset pulse inputs are provided using the push-button switches. It is observed that the circuit fails to work as desired. The SR latch can be made functional by changing **[2015]**



(A) NOR gates to NAND gates
(B) inverters to buffers
(C) NOR gates to NAND gates and inverters to buffers
(D) 5 V to ground

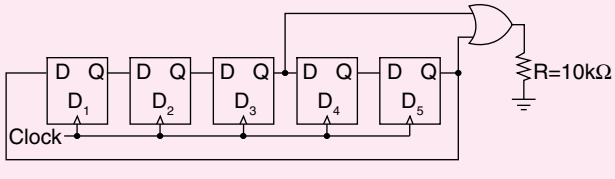
29. The block diagram of a frequency synthesizer consisting of a phase locked loop (PLL) and a divided by N counter (comprising ÷2, ÷4, ÷8, ÷16 outputs) (is sketched below. the synthesizer is excited with a 5 kHz signal (input 1). The free running frequency of the PLL is set to 20 kHz. Assume that the commutator switch makes contacts repeatedly in the order 1 – 2 – 3 – 4. **[2016]**



The corresponding frequencies synthesized are
(A) 10kHz, 20kHz, 40kHz, 80kHz
(B) 20kHz, 30kHz, 80kHz, 160kHz
(C) 80kHz, 40kHz, 20kHz, 10kHz
(D) 160kHz, 80kHz, 40kHz, 20kHz

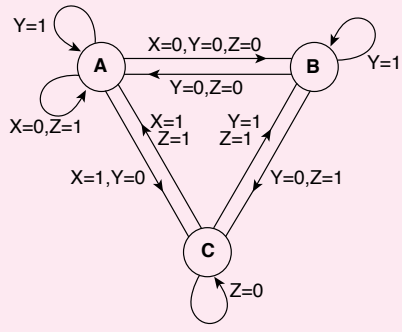
30. Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor R = 10 k Ω and the supply voltage is 5 V. The *D* flip flops D_1, D_2, D_3, D_4 and D_5 are initialized with logic values 0, 1, 0, 1, and 0, respectively. The clock has a 30% duty cycle.

[2016]



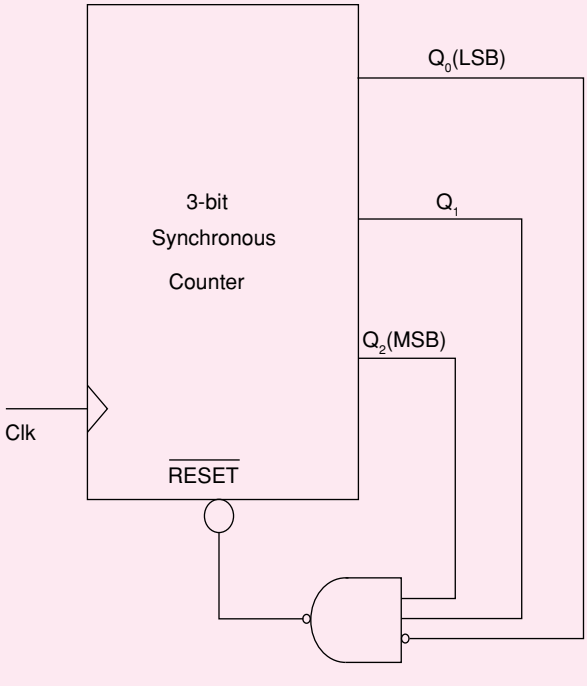
The average power dissipated (in mW) in the resistor *R* is _____.

31. The state transition diagram for a finite state machine with states A, B and C, and binary inputs X, Y and Z is shown in the figure **[2016]**



Which one of the following statements is correct?
(A) Transitions from state A are ambiguously defined.
(B) Transitions from State B are ambiguously defined.
(C) Transitions from State C are ambiguously defined.
(D) All of the state transitions are defined unambiguously.

32. For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero. **[2016]**



If the clock (CLK) frequency is 1 GHz, then the counter behaves as a
(A) mod – 5 counter
(B) mod 6 counter
(C) mod 7 counter
(D) mod 8 counter

Answer Keys

Exercises

Practice Problems 1

1. B	**2.** A	**3.** A	**4.** B	**5.** C	**6.** A	**7.** C	**8.** A	**9.** B	**10.** A
11. C	**12.** B	**13.** B	**14.** C	**15.** D	**16.** B	**17.** A	**18.** D	**19.** A	**20.** C
21. D	**22.** A	**23.** B	**24.** A	**25.** A					

Practice Problems 2

1. D	**2.** B	**3.** D	**4.** B	**5.** A	**6.** C	**7.** C	**8.** B	**9.** A	**10.** B
11. C	**12.** B	**13.** C	**14.** B	**15.** B	**16.** D	**17.** C	**18.** C	**19.** C	**20.** D
21. C	**22.** A	**23.** D	**24.** B	**25.** C	**26.** A	**27.** A	**28.** C	**29.** C	**30.** A

Previous Years' Questions

1. C	**2.** B	**3.** C	**4.** C	**5.** B	**6.** D	**7.** A	**8.** C	**9.** B	**10.** B
11. D	**12.** C	**13.** A	**14.** D	**15.** A	**16.** D	**17.** A	**18.** D	**19.** 62.4 to 62.6	
20. D	**21.** C	**22.** D	**23.** D	**24.** 7	**25.** C	**26.** A	**27.** D	**28.** A	**29.** A
30. 1.5mW		**31.** C	**32.** D						