Interrupts

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- When an interrupt is acknowledged the microprocessor perform following tasks:
  1. Microprocessor jumps a vectored location at page 00H where a subroutine (interrupt service routine) is written.
  2. Before jumping microprocessor saves the content of the program counter on the stack.
  3. It automatically resets the interrupt enable flip-flop.
- Interrupt which can be masked or stopped are maskable interrupt otherwise non-maskable interrupt. To mask and demask maskable interrupt of 8085 has to instruction i.e. EI and DI.
- Interrupt those vectored location is fixed are known as vectored interrupt otherwise non-vectored interrupt.

Hardware Interrupts

The 8085 microprocessor has five interrupt signals that can be used to interrupt a program execution.

Interrupt	Triggering	Vectored Address	Maskable/ Non-maskable
TRAP	Edge and level	0024H	Non-maskable
RST 7.5	Edge	002CH	Maskable
RST 6.5	Level	0034H	Maskable
RST 5.5	Level	003CH	Maskable
INTR	Level	Non vectored	Maskable

$\overline{INTA}$:

It is the active low interrupt acknowledgment signal which is only used with INTR.

Note:

Trick : Since it is a RST - 4.5,

So, $(4.5 \times 8)_{10} = (36)_{10} \xrightarrow{\text{Heaxadecimal}} (24)_H \approx (0024)_H$

Software Interrupt

There are 8 software interrupts which are used either in instructions or alongwith INTR interrupt. They are defined as RSTn where n → 0 to 7.

Software interrupt (RSTn)	Vectored address
RST 0	0000 H
RST 1	0008 H
RST 2	0010 H
RST 3	0018 H
RST 4	0020 H
RST 5	0028 H
RST 6	0030 H
RST 7	0038 H

Remember:

- TRAP is also called RST 4.5 interrupt.
- In interrupts priority order is
  TRAP > RST 7.5 > RST 6.5 > RST 5.5 > INTR
- Hold has higher priority than TRAP.
- RIM and SIM instructions are not only used for interrupt process but also used for serial I/O process.
- 8259A is a programmable interrupt controller and is used to implement and extend the capability of the 8085 interrupt. It manages 8 interrupt requests.

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