CHAPTER

2.3

THE BIPOLAR JUNCTION TRANSISTOR

Statement for Q.1-2:

The parameters in the base region of an *npn* bipolar transistor are as follows $D_n = 20\ \text{cm}^2/\text{s}$, $n_{B0} = 10^4\ \text{cm}^{-3}$, $x_B = 1\ \mu\text{m}$, $A_{BE} = 10^{-4}\ \text{cm}^2$.

1. If $V_{BE} = 0.5$ V, then collector current I_C is

(A) 7.75 μA (B) 1.6 μA

(C) 0.16 μA (D) 77.5 μA

2. If $V_{BE} = 0.7$ V, then collector current I_C is

(A) 418 μA (B) 210 μA

(C) 17.5 μA (D) 98 μA

3. In bipolar transistor biased in the forward-active region the base current is $I_B = 50\ \mu\text{A}$ and the collector currents is $I_C = 2.7$ mA. The α is

(A) 0.949 (B) 54

(C) 0.982 (D) 0.018

4. A uniformly doped silicon *npn* bipolar transistor is to be biased in the forward active mode with the B-C junction reverse biased by 3 V. The transistor doping are $N_E = 10^{17}\ \text{cm}^{-3}$, $N_B = 10^{16}\ \text{cm}^{-3}$ and $N_C = 10^{15}\ \text{cm}^{-3}$. The BE voltage, at which the minority carrier electron concentration at $x = 0$ is 10% of the majority carrier hole concentration, is

(A) 0.94 V (B) 0.64 V

(C) 0.48 V (D) 0.24 V

5. A uniformly doped *npn* bipolar transistor is biased in the forward-active region. The transistor doping concentration are $N_E = 5 \times 10^{17}\ \text{cm}^{-3}$, $N_B = 10^{16}\ \text{cm}^{-3}$ and $N_C = 10^{15}\ \text{cm}^{-3}$. The minority carrier concentration p_{E0}, n_{B0} and p_{C0} are

(A) 4.5×10^2, 2.25×10^4, $2.25 \times 10^5\ \text{cm}^{-3}$

(B) 2.25×10^4, 2.25×10^5, $4.5 \times 10^2\ \text{cm}^{-3}$

(C) 2.25×10^4, 2.25×10^5, $4.5 \times 10^4\ \text{cm}^{-3}$

(D) 4.5×10^4, 2.25×10^4, $2.25 \times 10^5\ \text{cm}^{-3}$

6. A uniformly doped silicon *pnp* transistor is biased in the forward-active mode. The doping profile is $N_E = 10^{18}\ \text{cm}^{-3}$, $N_B = 5 \times 10^{16}\ \text{cm}^{-3}$ and $N_C = 10^{15}\ \text{cm}^{-3}$. For $V_{EB} = 0.6$ V, the p_B at $x = 0$ is (See fig. P2.3.7-8)

(A) $5.2 \times 10^{19}\ \text{cm}^{-3}$ (B) $5.2 \times 10^{13}\ \text{cm}^{-3}$

(C) $5.2 \times 10^{16}\ \text{cm}^{-3}$ (D) $5.2 \times 10^{11}\ \text{cm}^{-3}$

Statement for Q.7-8:

An *npn* bipolar transistor having uniform doping of $N_E = 10^{18}\ \text{cm}^{-3}$ $N_B = 10^{16}\ \text{cm}^{-3}$ and $N_C = 6 \times 10^{15}\ \text{cm}^{-3}$ is operating in the inverse-active mode with $V_{BE} = -2$ V and $V_{BC} = 0.6$ V. The geometry of transistor is shown in fig P2.3.7-8.

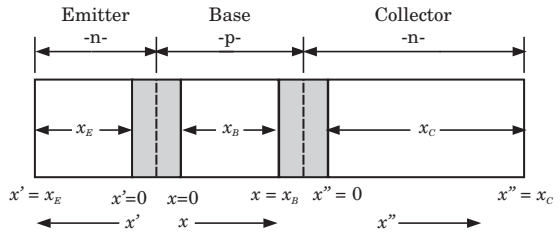

Fig. P2.3.7-8

7. The minority carrier concentration at $x = x_B$ is

(A) 4.5×10^{14} cm^{-3} (B) 2.6×10^{12} cm^{-3}

(C) 2.6×10^{14} cm^{-3} (D) 3.9×10^{14} cm^{-3}

8. The minority carrier concentration at $x'' = 0$ is

(A) 3.9×10^{14} cm^{-3} (B) 2.7×10^{12} cm^{-3}

(C) 2.7×10^{14} cm^{-3} (D) 4.5×10^{14} cm^{-3}

9. An *pnp* bipolar transistor has uniform doping of $N_E = 6 \times 10^{17}$ cm^{-3}, $N_B = 2 \times 10^{16}$ cm^{-3} and $N_C = 5 \times 10^{14}$ cm^{-3}. The transistor is operating is inverse-active mode. The maximum V_{CB} voltage, so that the low injection condition applies, is

(A) 0.86 V (B) 0.48 V

(C) 0.32 V (D) 0.60 V

Statement for Q.10-12:

The following currents are measured in a uniformly doped *npn* bipolar transistor:

$I_{nE} = 1.20$ mA, $I_{pE} = 0.10$ mA, $I_{nC} = 1.18$ mA

$I_R = 0.20$ mA, $I_G = 1\,\mu$A, $I_{pC0} = 1\,\mu$A

10. The α is

(A) 0.667 (B) 0.733

(C) 0.787 (D) 0.8

11. The β is

(A) 3.69 (B) 0.44

(C) 2.27 (D) 8.39

12. The γ is

(A) 0.816 (B) 0.923

(C) 1.083 (D) 0.440

13. A silicon *npn* bipolar transistor has doping concentration of $N_E = 2 \times 10^{18}$ cm^{-3}, $N_B = 10^{17}$ cm^{-3} and $N_C = 1.5 \times 10^{16}$ cm^{-3}. The area is 10^{-3} cm^2 and neutral base width is 1 μm. The transistor is biased in the active region at $V_{BE} = 0.5$ V. The collector current is

($D_B = 20$ cm^2/s)

(A) 9 μA (B) 17 μA

(C) 22 μA (D) 11 μA

14. A uniformly doped *npn* bipolar transistor has following parameters:

$N_E = 10^{18}$ cm^{-3}, $N_B = 5 \times 10^{16}$ cm^{-3},

$N_C = 2 \times 10^{19}$ cm^{-3},

$D_E = 8$ cm^2/s , $D_B = 15$ cm^2/s , $D_C = 14$ cm^2/s

$x_E = 0.8\,\mu$m, $x_B = 0.7\,\mu$m

The emitter injection efficiency γ is

(A) 0.999 (B) 0.977

(C) 0.982 (D) 0.934

15. A uniformly doped silicon epitaxial *npn* bipolar transistor is fabricated with a base doping of $N_B = 3 \times 10^{16}$ cm^{-3} and a heavily doped collector region with $N_C = 5 \times 10^{17}$ cm^{-3}. The neutral base width is $x_B = 0.7\,\mu$m when $V_{BE} = V_{BC} = 0$. The V_{BC} at punch-through is

(A) 26.3 V (B) 18.3 V

(C) 12.2 V (D) 6.3 V

16. A silicon *npn* transistor has a doping concentration of $N_B = 10^{17}$ cm^{-3} and $N_C = 7 \times 10^{15}$ cm^{-3}. The metallurgical base width is 0.5 μm. Let $V_{BE} = 0.6$ V. Neglecting the B–E junction depletion width the V_{CE} at punch-through is

(A) 146 V (B) 70 V

(C) 295 V (D) 204 V

17. A uniformly doped silicon *pnp* transistor is to designed with $N_E = 10^{19}$ cm^{-3} and $N_C = 10^{16}$ cm^{-3}. The metallurgical base width is to be 0.75 μm. The minimum base doping, so that the minimum punch-through voltage is $V_{pt} = 25$ V, is

(A) 4.46×10^{15} cm^{-3} (B) 4.46×10^{16} cm^{-3}

(C) 1.95×10^{15} cm^{-3} (D) 1.95×10^{16} cm^{-3}

18. For a silicon *npn* transistor assume the following parameters:

$I_E = 0.5$ mA, $\beta = 48$

$x_B = 0.7\,\mu$A, $x_{dc} = 2\,\mu$m

$C_s = C_\mu = 0.08$ pF, $C_{je} = 0.8$ pF

$D_n = 25$ cm^2/s, $r_c = 30\,\Omega$

The carrier cross the space charge region at a speed of 10^7 cm/s. The total delay time τ_{ec} is

(A) 164.2 ps (B) 234.4 ps

(C) 144.2 ps (D) 298.4 ps

19. In a bipolar transistor, the base transit time is 25% of the total delay time. The base width is 0.5 μm and base diffusion coefficient is $D_B = 20\ \text{cm}^2/\text{s}$. The cut-off frequency is

(A) 637 MHz (B) 436 MHz

(C) 12.8 GHz (D) 46.3 GHz

20. The base transit time of a bipolar transistor is 100 ps and carriers cross the 1.2 μm B–C space charge at a speed of 10^7 cm/s . The emitter-base junction charging time is 25 ps and the collector capacitance and resistance are 0.10 pF and 10 Ω, respectively. The cutoff frequency is

(A) 43.8 GHz (B) 32.6 GHz

(C) 3.26 GHz (D) 1.15 GHz

Statement for Q.21-22:

Consider the circuit shown in fig. P2.3.21-22. If voltage $V_s = 0.63\text{V}$, the currents are $I_C = 275\ \mu\text{A}$ and $I_B = 5\ \mu\text{A}$.

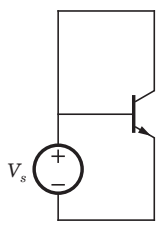

Fig.P2.3.21-22

21. The forward common-emitter gain β_F is

(A) 56 (B) 55

(C) 0.9821 (D) 0.9818

22. The forward current gain α_F is

(A) 0.9821 (B) 0.9818

(C) 55 (D) 56

23. Consider the circuit shown in fig P2.3.23. If $V_s = 0.63$ V, $I_1 = 275\ \mu\text{A}$ and $I_2 = 125\ \mu\text{A}$, then the value of I_3 is

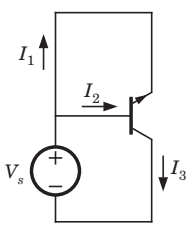

Fig. P2.3.23

(A) – 400 μA (B) 400 μA

(C) – 600 μA (D) 600 μA

Statement for Q.24-26:

For the transistor in circuit of fig. P2.3.24-26. The parameters are $\beta_R = 1, \beta_F = 100$, and $I_s = 1$ fA .

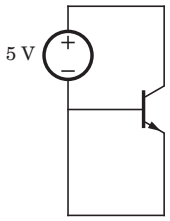

Fig. P2.3.24-26

24. The current I_C is

(A) 1 fA (B) 2 fA

(C) 1.384 fA (D) 0 A

25. The current I_E is

(A) 1 fA (B) -1 fA

(C) 2 fA (D) -2 fA

26. The current I_B is

(A) 2 fA (B) -2 fA

(C) 1 fA (D) -1 fA

27. For the transistor in fig. P2.3.27, $I_S = 10^{-15}$ A, $\beta_F = 100$, $\beta_R = 1$. The current I_{CBO} is

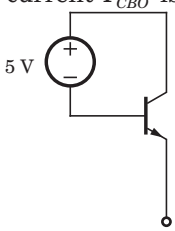

Fig.P2.3.27

(A) 1.01×10^{-14} A (B) 2×10^{-14} A

(C) 1.01×10^{-15} A (D) 2×10^{-15} A

Statement for Q.28-31:

Determine the region of operation for the transistor shown in circuit in question.

28.

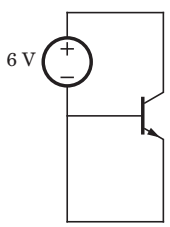

Fig.P2.3.28

(A) Forward-Active (B) Reverse-Active

(C) Saturation (D) Cutoff

29.

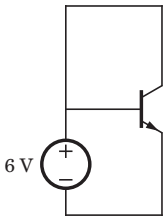

Fig. P2.3.29

(A) Forward-Active (B) Reverse-Active

(C) Saturation (D) Cutoff

30.

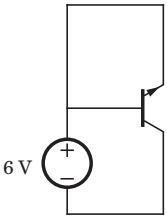

Fig.P2.3.30

(A) Forward-Active (B) Reverse-Active

(C) Saturation (D) Cutoff

31.

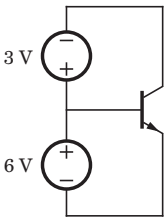

Fig.P2.3.31

(A) Forward-Active (B) Reverse-Active

(C) Saturation (D) Cutoff

Statement for Q.32-33:

For the circuit shown in fig. P2.3.32-33, let the value of $\beta_R = 0.5$ and $\beta_F = 50$. The saturation current is 10^{-16} A.

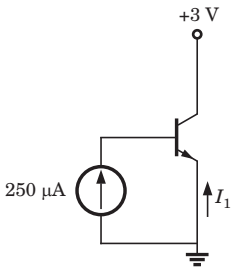

Fig. P2.3.32-33

32. The base-emitter voltage is

(A) 0.53 V (B) 0.7 V

(C) 0.84 V (D) 0.98 V

33. The current I_1 is

(A) –12.75 mA (B) 12.75 mA

(C) 12.5 mA (D) – 12.5 mA

Statement for Q.34–35:

The leakage current of a transistor are $I_{CBO} = 5$ μA and $I_{CEO} = 0.4$ mA, and $I_B = 30$ μA.

34. The value of β is

(A) 79 (B) 81

(C) 80 (D) None of the above

35. The value of I_C is

(A) 2.4 mA (B) 2.77 mA

(C) 2.34 mA (D) 1.97 mA

Statement for Q.36–37:

For a BJT, $I_C = 5$ mA, $I_B = 50$ μA and $I_{CBO} = 0.5$ μA.

36. The value of β is

(A) 103 (B) 91

(C) 83 (D) 51

37. The value of I_E is

(A) 5.25 mA (B) 5.4 mA

(C) 5.65 mA (D) 5.1 mA

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SOLUTIONS

1. (A) $I_C = I_s e^{\left(\frac{V_{BE}}{V_b}\right)}$

$$I_s = \frac{eD_n A_{BE} n_{B0}}{x_B}$$

$$= \frac{(1.6\times10^{-19})(20)(10^{-4})(10^{4})}{10^{-4}} = 3.2\times10^{-14}\ \text{A}$$

$$I_C = 3.2\times10^{-14} e^{\left(\frac{0.5}{0.0259}\right)} = 7.75\ \mu\text{A}$$

2. (C) $I_C = 3.2\times10^{-14} e^{\left(\frac{0.7}{0.0259}\right)} = 17.5\ \text{mA}$

3. (C) $\beta_F = \frac{I_C}{I_B}$, $\alpha_F = \frac{\beta_F}{1+\beta_F}$

$$\alpha_F = \frac{I_C}{I_C + I_B} = \frac{2.7\text{m}}{2.7\text{m} + 50\mu} = 0.982$$

4. (B) $n_{p0} = \frac{n_i^2}{N_B} = \frac{(1.5\times10^{10})^2}{10^{16}} = 2.25\times10^{4}\ \text{cm}^{-3}$

At $x = 0$, $n_p(0) = n_{p0} e^{\left(\frac{V_{BE}}{V_t}\right)}$

$$\Rightarrow \quad V_{BE} = V_T \ln\left(\frac{n_p(0)}{n_{p0}}\right)$$

$$n_p(0) = \frac{10}{100}\times N_B = \frac{10^{16}}{10} = 10^{15}$$

$$V_{BE} = 0.0259 \ln\left(\frac{10^{15}}{2.25\times10^{4}}\right) = 0.635\ \text{V}$$

5. (A) $p_{E0} = \frac{n_i^2}{N_E} = \frac{(1.5\times10^{10})^2}{5\times10^{17}} = 450\ \text{cm}^{-3}$

$$n_{B0} = \frac{n_i^2}{N_B} = \frac{(1.5\times10^{10})^2}{5\times10^{16}} = 2.25\times10^{4}\ \text{cm}^{-3}$$

$$p_{C0} = \frac{n_i^2}{N_E} = \frac{(1.5\times10^{10})^2}{5\times10^{15}} = 2.25\times10^{5}\ \text{cm}^{-3}$$

6. (B) $p_{B0} = \frac{n_i^2}{N_B} = \frac{(1.5\times10^{10})^2}{5\times10^{16}} = 4.5\times10^{3}\ \text{cm}^{-3}$

$$p_B(0) = p_{B0} e^{\left(\frac{V_{EB}}{V_t}\right)} = 4.5\times10^{3} e^{\left(\frac{0.6}{0.0259}\right)} = 5.2\times10^{13}\ \text{cm}^{-3}$$

7. (C) $n_{B0} = \frac{n_i^2}{N_B} = \frac{(1.5\times10^{10})^2}{10^{16}} = 2.25\times10^{4}\ \text{cm}^{-3}$

$$n_B(x = x_B) = n_{B0} e^{\left(\frac{V_{BC}}{V_t}\right)}$$

$$= 2.25\times10^{4} e^{\frac{0.6}{0.0259}} = 2.6\times10^{14}\ \text{cm}^{-3}$$

8. (D) $p_{C0} = \frac{n_i^2}{N_C} = \frac{(1.5\times10^{10})^2}{6\times10^{15}} = 3.75\times10^{4}\ \text{cm}^{-3}$

$$p_C(x'' = 0) = p_{C0} e^{\left(\frac{V_{BC}}{V_t}\right)}$$

$$= 3.75\times10^{4} e^{\left(\frac{0.6}{0.0259}\right)} = 4.31\times10^{14}\ \text{cm}^{-3}$$

9. (B) Low injection limit is reached when $p_C(0) = 0.10 N_C = 5\times10^{13}\ \text{cm}^{-3}$,

$$p_{C0} = \frac{n_i^2}{N_C} = \frac{(1.5\times10^{10})^2}{5\times10^{14}} = 4.5\times10^{5}$$

$$p_C(0) = p_{C0} e^{\left(\frac{V_{CB}}{V_t}\right)} \quad \Rightarrow \quad V_{CB} = V_t \ln\left(\frac{p_C(0)}{p_{C0}}\right)$$

$$= 0.0259 \ln\left(\frac{5\times10^{13}}{4.5\times10^{5}}\right) = 0.48\ \text{V}$$

10. (C) $\alpha = \frac{J_{nC}}{J_{nE} + J_R + J_{pE}} = \frac{I_{nC}}{I_{nE} + I_R + I_{pE}}$

$$= \frac{1.18}{1.2 + 0.2 + 0.1} = 0.787$$

11. (A) $\beta = \frac{\alpha}{1-\alpha} == \frac{0.787}{1-0.787} = 3.69$

12. (B) $\gamma = \frac{J_{nE}}{J_{nE} + J_{pE}} = \frac{I_{nE}}{I_{nE} + I_{pE}} = \frac{1.2}{1.2 + 0.1} = 0.923$

13. (B) $n_{B0} = \frac{n_i^2}{N_B} = \frac{(1.5\times10^{10})^2}{10^{17}} = 2.25\times10^{3}\ \text{cm}^{-3}$

$$n_B(0) = n_{B0} e^{\left(\frac{V_{BE}}{V_t}\right)} = 2.25\times10^{3} e^{\left(\frac{0.5}{0.0259}\right)} = 5.45\times10^{11}\ \text{cm}^{-3}$$

$$I_C = \frac{eD_B A n_B(0)}{x_B}$$

$$= \frac{(1.6\times10^{-19})(20)(10^{-3})(5.45\times10^{11})}{10^{-4}} = 17.4\ \mu\text{A}$$

14. (B) $\gamma = \frac{1}{1 + \frac{N_B}{N_E}\cdot\frac{D_E}{D_B}\cdot\frac{x_B}{x_E}}$

$$= \frac{1}{1 + \frac{5\times10^{16}}{10^{18}}\frac{8}{15}\frac{0.7}{0.8}} = 0.977$$

15. (B) $V_{bi} = V_t \ln\left(\frac{N_B N_C}{n_i^2}\right)$

$$= 0.0259 \ln\left(\frac{3\times10^{16}\times5\times10^{17}}{(1.5\times10^{10})^2}\right) = 0.824\ \text{V}$$

At punch-through

27. (C) $I_E = I_S\left(e^{\left(\frac{V_{BE}}{V_t}\right)} - e^{\left(\frac{V_{BC}}{V_t}\right)}\right) + \frac{I_S}{\beta_F}\left(e^{\left(\frac{V_{BE}}{V_t}\right)} - 1\right) = 0$

$$\Rightarrow \quad e^{\left(\frac{V_{BE}}{V_t}\right)} = \frac{1}{1+\beta_F} + \frac{\beta_R}{1+B_F} e^{\left(\frac{V_{BC}}{V_t}\right)}$$

$$I_C = I_S\left[e^{\left(\frac{V_{BE}}{V_t}\right)} - e^{\left(\frac{V_{BC}}{V_t}\right)}\right] - \frac{I_S}{\beta_R}\left[e^{\left(\frac{V_{BC}}{V_t}\right)} - 1\right]$$

$$I_{CBO} = \frac{I_S}{1+\beta_F}\left[1 - e^{\left(\frac{V_{BC}}{V_t}\right)}\right] - \frac{I_S}{\beta_R}\left[e^{\left(\frac{V_{BC}}{V_t}\right)} - 1\right]$$

$V_{BC} = -5$ V, $V_t = 0.0259$ V

$$I_{CBO} = \frac{I_s}{101}(1-0) - \frac{I_S}{1}(0-1) = 1.01 I_S = 1.01 \times 10^{-15} \text{ A}$$

28. (D)

B-E junction V_{BE}	B-C Junction V_{BC}	
	Reverse Bias	Forward bias
Forward bias	Forward-Active	Saturation
Reverse Bias	Cut-off	Reverse-Active

$V_{BE} = 0$, $V_{BC} < 0$, Thus both junction are in reverse bias. Hence cutoff region.

29.(A) $V_{BE} > 0$, $V_{BC} = 0$, Base-Emitter junction forward bais, Base-collector junction reverse bias, Hence forward-active region.

30. (B) $V_{BE} = 0$, $V_{BC} > 0$, Base-Emitter junction reverse bais , Base-collector junction forward bias, Hence reverse-active region.

31. (C) $V_{BE} = 6$ V, $V_{BC} = 3$ V, Both junction are forward biase, Hence saturation region.

32. (C) The current source will forward bias the base-emitter junction and the collector base junction will then be reverse biased. Therefore the transistor is in the forward active region

$$I_C = I_S e^{\left(\frac{V_{BE}}{V_t}\right)}$$

$$I_C = \beta_F I_B = 50 \times 250 \times 10^{-6} = 12.5 \times 10^{-3} \text{ A}$$

$$V_{BE} = V_t \ln\left(\frac{I_C}{I_S}\right) = 0.0259 \ln\left(\frac{12.5 \times 10^{-3}}{10^{-16}}\right) = 0.84 \text{ V}$$

33. (A) $I_E = (\beta_F + 1) I_B = 12.75$ mA

$I_1 = -I_E = -12.75$ mA.

34. (A) $I_{CEO} = (\beta + 1) I_{CBO}$

$$\beta + 1 = \frac{0.4\text{m}}{5\mu} = 80 \quad \Rightarrow \quad \beta = 79$$

35. (B) $I_C = \beta I_B + I_{CEO} = 79(30\mu) + 0.4\text{m} = 2.77$ mA

36. (A) $I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$

$$\beta = \frac{I_C - I_{CBO}}{I_B + I_{CBO}} = \frac{5.2\text{m} - 0.5\mu}{50\mu + 0.5\mu} \approx 103.96$$

37. (A) $\alpha = \frac{\beta}{\beta + 1} = 0.9904$

$$I_E = \frac{I_C - I_{CBO}}{\alpha} = \frac{5.2\text{m} - 0.5\mu}{0.9904} = 5.25 \text{ MA}$$

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11. In n-well CMOS fabrication substrate is

(A) lightly doped n – type

(B) lightly doped p – type

(C) heavily doped n – type

(D) heavily doped p – type

12. The chemical reaction involved in epitaxial growth in IC chips takes place at a temperature of about

(A) 500° C (B) 800° C

(C) 1200° C (D) 2000° C

13. A single monolithic IC chip occupies area of about

(A) 20 mm^2 (B) 200 mm^2

(C) 2000 mm^2 (D) 20,000 mm^2s

14. Silicon dioxide layer is used in IC chips for

(A) providing mechanical strength to the chip

(B) diffusing elements

(C) providing contacts

(D) providing mask against diffusion

15. The p-type substrate in a monolithic circuit should be connected to

(A) any dc ground point

(B) the most negative voltage available in the circuit

(C) the most positive voltage available in the circuit

(D) no where, i.e. be floating

16. The collector-substrate junction in the epitaxial collector structure is, approximately

(A) a step-graded junction

(B) a linearly graded junction

(C) an exponential junction

(D) None of the above

17. The sheet resistance of a semiconductor is

(A) an important characteristic of a diffused region especially when used to form diffused resistors

(B) an undesirable parasitic element

(C) a characteristic whose value determines the required area for a given value of integrated capacitance

(D) a parameter whose value is important in a thin-film resistance

18. Monolithic integrated circuit system offer greater reliability than discrete-component systems because

(A) there are fewer interconnections

(B) high-temperature metalizing is used

(C) electric voltage are low

(D) electric elements are closely matched

19. Silicon dioxide is used in integrated circuits

(A) because of its high heat conduction

(B) because it facilitates the penetration of diffusants

(C) to control the location of diffusion and to protect and insulate the silicon surface.

(D) to control the concentration of diffusants.

20. Increasing the yield of an IC

(A) reduces individual circuit cost

(B) increases the cost of each good circuit

(C) results in a lower number of good chips per wafer

(D) means that more transistor can be fabricated on the same size wafer.

21. The main purpose of the metalization process is

(A) to act as a heat sink

(B) to interconnect the various circuit elements

(C) to protect the chip from oxidation

(D) to supply a bonding surface for mounting the chip

22. In a monolithic-type IC

(A) each transistor is diffused into a separate isolation region

(B) all components are fabricated into a single crystal of silicon

(C) resistors and capacitors of any value may be made

(D) all isolation problems are eliminated

23. Isolation in ICs is required

(A) to make it simpler to test circuits

(B) to protect the transistor from possible ``thermal run away"

(C) to protect the components mechanical damage

(D) to minimize electrical interaction between circuit components

24. Almost all resistor are made in a monolithic IC

(A) during the base diffusion

(B) during the collector diffusion

(C) during the emitter diffusion

(D) while growing the epitaxial layer

25. The equation governing the diffusion of neutral atom is

(A) $\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2}$ (B) $\frac{\partial N}{\partial x} = D \frac{\partial^2 N}{\partial t^2}$

(C) $\frac{\partial^2 N}{\partial t^2} = D \frac{\partial N}{\partial x}$ (D) $\frac{\partial^2 N}{\partial x^2} = D \frac{\partial N}{\partial t}$

26. The true statement is

(A) thick film components are vacuum deposited

(B) thin film component are made by screen-and- fire process

(C) thin film resistor have greater precision and are more stable

(D) thin film resistor are cheaper than the thin film resistor

27. The False statement is

(A) Capacitor of thin film capacitor made with proper dielectric is not voltage dependent

(B) Thin film resistors and capacitor need to be biased for isolation purpose

(C) Thin film resistors and capacitor have smaller stray capacitances and leakage currents.

(D) None of the above

28. Consider the following two statements

S_1 : The dielectric isolation method is superior to junction isolation method.

S_2 : The beam lead isolation method is inferior to junction isolation method.

The true statements is (are)

(A) S_1 , S_2 (B) only

(C) only (D) Neither nor S_2

29. If P is passivation, Q is n-well implant, R is metallization and S is source/drain diffusion, then the order in which they are carried out in a standard n-well CMOS fabrication process is

(A) S - R - Q - P (B) R - P - S - Q

(C) Q - S - R - P (D) P - Q - R - S

30. For the circuit shown in fig. P2.5.30, the minimum number and the maximum number of isolation regions are respectively

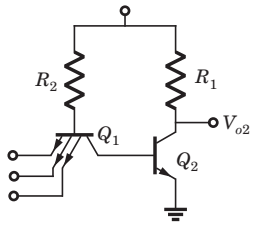

Fig. P2.5.32

(A) 2, 6 (B) 3, 6

(C) 2, 4 (D) 3, 4

31. For the circuit shown in fig. P2.5.31, the minimum number of isolation regions are

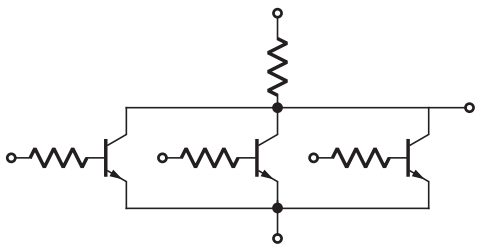

Fig. P2.5.31

(A) 2 (B) 3

(C) 4 (D) 7

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SOLUTIONS

1. (D)	2. (D)	3. (B)	4. (B)	5. (C)	6. (B)
7. (C)	8. (B)	9. (C)	10. (D)	11. (B)	12. (C)
13. (C)	14. (D)	15. (B)	16. (A)	17. (A)	18. (A)
19. (C)	20. (A)	21. (B)	22. (B)	23. (D)	24. (A)
25. (A)	26. (C)	27. (B)	28. (B)	29. (C)	

30. (D) The minimum number of isolation region is 3 one containing Q_1 , one containing and one containing both and . The maximum number of isolation region is 4, or one per component.

31. (A) The minimum number of isolation region is two. One for transistor and one for resistor.

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