Chapter 3

Field Effect Transistors

LEARNING OBJECTIVES

After reading this chapter, you will be able to understand:

- JFET
- Parameters of FET
- Relation between BJT and JFET
- Comparisons of JFET and BJT
- Introduction to MOSFET
- D–MOSFET
- E–MOSFET
- The body effect
- N–MOS transistor
- PMOS transistors
- Conditions for saturation region

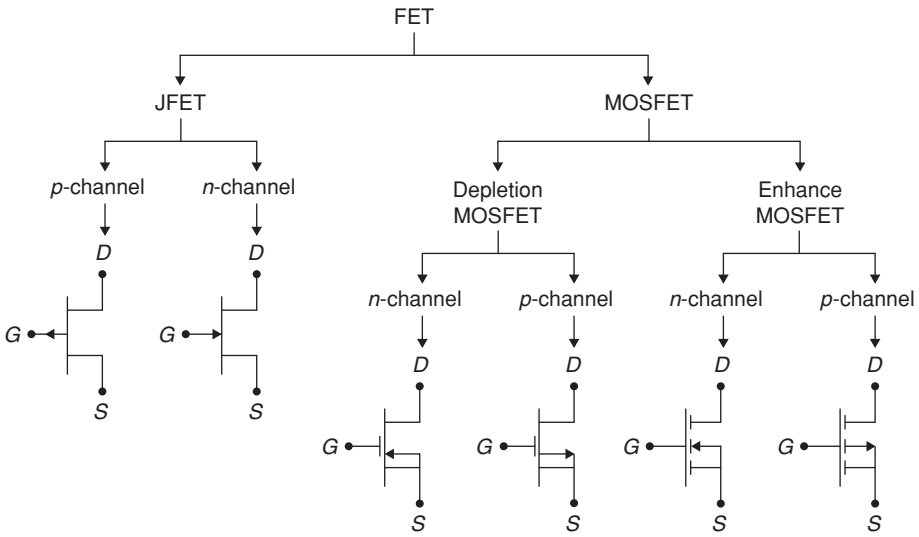
Introduction

The bipolar junction transistor relies on two types of charge carriers i.e., free electrons and holes. Another kind of transistor is called the field effect transistor (FET). This type of device is unipolar because its operation depends on only one type of charge, either free electrons or holes. In other words, an FET has majority carriers but not minority carriers.

The FET is generally much less noisy than the BJT. BJT is a current controlled device, and FET is a voltage controlled current device.

These are two types:

1. Junction field effect transistors (JFET).
2. Metal oxide semiconductor field effect transistor (MOSFET).



JFET

A junction field effect transistor (see Figure 1) is a three terminal semiconductor device in which current conduction is by majority types of carriers i.e., electrons or holes. JFET has high input impedance and low noise level.

Construction of JFET

A junction field effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.

A JFET consists of a *p*-type or *n*-type silicon material, containing two *p*-*n* junctions at the sides. If the bar is *n*-type, it is called a *n*-channel JFET and if the bar is of *p*-type, it is called a *p*-channel JFET.

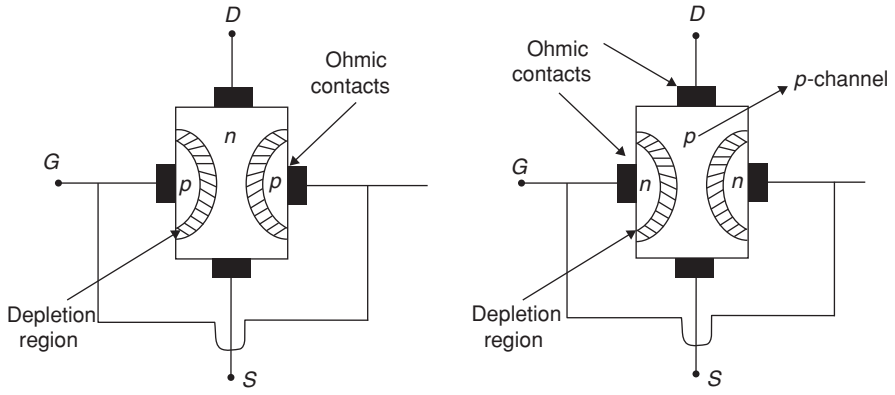


Figure 1 Junction field effect transistors.

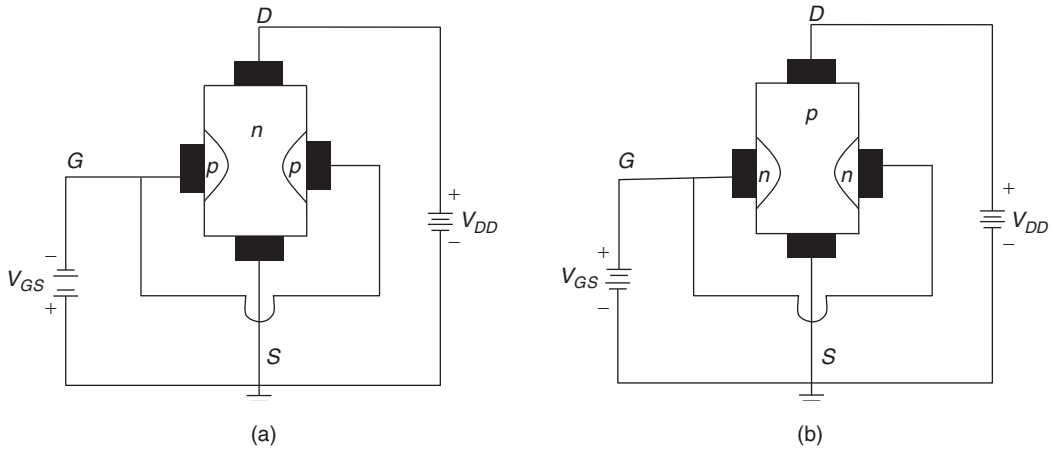


Figure 2 JFET polarities. (a) *n*-channel JFET, (b) *p*-channel JFET

The input circuit (gate to source) of a JFET is reverse biased and output circuit (drain to source) of a JFET is forward bias, i.e., the device has high input impedance and low output impedance.

Working Principle

The two *p*–*n* junctions at the sides form two depletion layers. The current conduction by charge carriers (majority carriers) is through the channel between the two depletion layers and out of the drain. The width of the channel, i.e., resistance of this channel can be controlled by changing the input voltage V_{GS}.

The reverse voltage V_{GS} increases, the wider will be the depletion layers and narrower will be the conduction channel i.e., channel width decreases means resistance of the channel increases, so drain to source current decreases. Otherwise the reverse will be happen when V_{GS} decreases.

Thus, JFET operates on the principle that width and resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.

***Case* (1):** For *n*-channel JFET

$$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V}$$

In this case drain current $I_D = 0$, because $V_{DS} = 0$ V.

***Case* (2):** When $V_{GS} = 0$ V and V_{DS} some +ve value

As the voltage V_{DS} is increased from 0 V to a few Volts, the current will increase as determined by ohm's law and the characteristics plot of $I_D V_S V_{DS}$ shown in Figure 4.

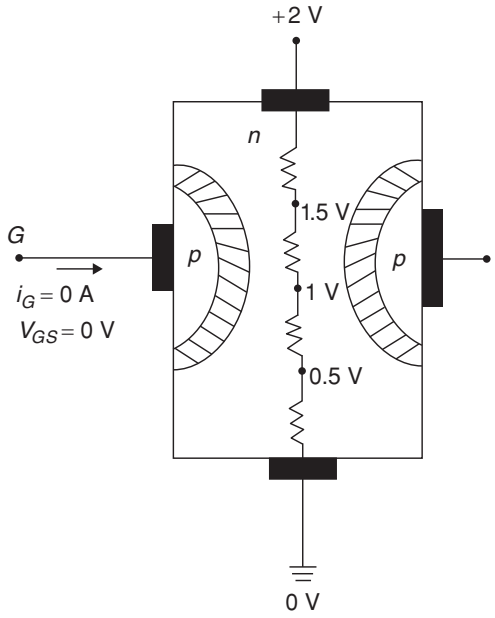


Figure 3 Varying reverse bias potential across the *p-n* junction of an *n*-channel JFET.

I–V Characteristics

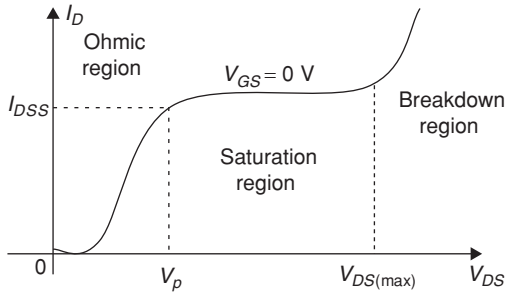


Figure 4 I_D vs. V_{DS} for V_{GS} = 0 V

The ohmic relationship between V_{DS} and I_D continues till V_{DS} reaches a certain critical value is called pinch off voltage (V_p).

If the drain voltage exceeds $V_{DS(max)}$, JFET enters into break down region.

The region between the V_P and $V_{DS(max)}$ is called constant current region because when V_{DS} equal to V_P, the channel is effectively closed and does not allow further increase in drain current shown in Figure 5.

***Case* (3):** If $V_{GS} < 0$ and V_{DS} = Constant

If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other at $|V_{GS(off)}| = |V_P|$ and the channel is cut-off.

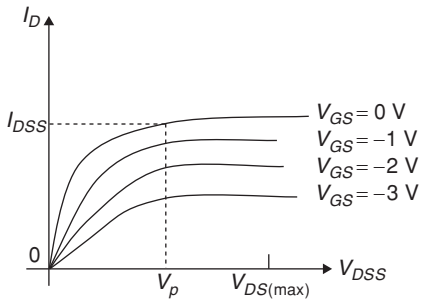
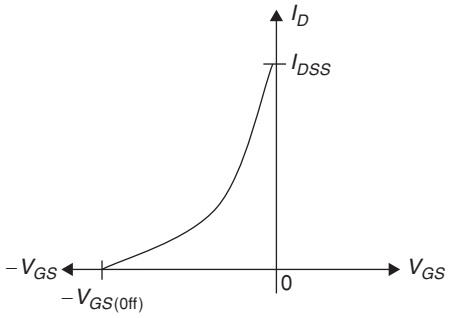


Figure 5 *n*-channel JFET characteristics.



***Shorted-gate drain current* (I_{DSS})** It is the drain current with source, short circuited to gate ($V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage. It is the maximum drain current (I_{DSS}). The region between V_P and $V_{DS(max)}$ (break down voltage) is called constant-current region or saturation region. JFET behaves as a constant-current device. For proper working of JFET, it must be operated in the saturation region or active mode.

***Pinch off Voltage* (V_P)** It is the minimum drain-source voltage at which the drain current becomes constant. For values of V_{DS} greater than V_P, the drain current is almost constant. Because when V_{DS} is equal to V_P, the channel is effectively closed and does not allow further increase in drain current. However, V_{DS} should not exceed $V_{DS(max)}$ otherwise JFET may break down.

***Gate-source cut-off Voltage* $V_{GS(off)}$** It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero. As the reverse gate-source voltage is increased, the cross sectional area of the channel decreases. This in turn decreases the drain current. At some gate to source voltage, the depletion region is increased and touches each other. In this condition, the channel is cut off and the drain current reduces to zero.

$$V_P = |V_{GS(off)}|$$

Parameters of GFET

Drain current (I_D)

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \text{A}$$

Where

I_D = drain current at given V_{GS}

I_{DSS} = short circuit gate drain current

V_{GS} = gate-source voltage

V_P = gate-source cut-off voltage (or) pinch off voltage

Drain resistance (r_d)

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}; \text{ at constant } V_{GS}$$

The drain resistance of a JFET has a large value range from 10 kΩ to 1 MΩ.

Transconductance (g_m)

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}.$$

Amplification factor (μ)

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in the gate to source voltage (ΔV_{GS})

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}; \text{ at constant } I_D.$$

Relation among JFET parameters

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \times g_m$$

$\therefore \mu = g_m \cdot r_d$

$$g_m = g_{m_o}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Where,

$$g_{m_o} = \frac{2I_{DSS}}{|V_P|} \text{ or } \frac{-2I_{DSS}}{V_P}$$

Or

$$g_m = g_{m_o} \cdot \sqrt{\frac{I_D}{I_{DSS}}}$$

DC drain resistance, $R_{DS} = \frac{V_{DS}}{I_D}$

voltage gain $A_V = -g_m \cdot R_D$

Solved Examples

Example 1: A JFET has $V_p = -4.5$ V, $I_{DSS} = 10$ mA and $I_D = 2.5$ mA. Determine the transconductance.

Solution: $g_m = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_P}\right]$

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= 2.22 \text{ mA/V}$$

Example 2: For an *n*-channel JFET $I_{DSS} = 8.7$ mA, $V_p = -3$ V, $V_{GS} = -1$ V. Find the values of

(A) I_D (B) g_{m_0} (C) g_m

Solution:

(A) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 3.8667$ mA

(B) $g_{m_0} = \frac{-2I_{DSS}}{V_P} = 5.8$ mA/V

(C) $g_m = g_{m_0}\left(1 - \frac{V_{GS}}{V_P}\right) = 3.867$ mA/V

Example 3: For a *n*-channel JFET, $I_{DSS} = 8$ mA, $V_p = -4$ V, $V_{GS} = -1$ V. Determine I_D, g_{m_o} and g_m.

Solution: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$$= 8 \times 10^{-3}\left(1 - \frac{(-1)}{(-4)}\right)^2$$

$$I_D = 4.5 \text{ mA}$$

$$g_{m_o} = \frac{-2I_{DSS}}{V_p}$$

$$= 4 \text{ mA/V}$$

$$g_m = g_{m_o}\left(1 - \frac{V_{GS}}{V_p}\right) = 3 \text{ mA/V}.$$

Example 4: In a JFET, the drain current is changed by 0.25 mA when the gate to source voltage is changed by 0.25 V, keeping drain-source voltage constant. Calculate the transconductance of the JFET.

Solution: $g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{constant}}$

$$= \frac{0.25 \times 10^{-3}}{0.125}$$

$$g_m = 2 \text{ mA/V}.$$

Example 5: A JFET has $g_m = 10$ ms, $I_{DSS} = 10$ μA. Calculate $V_{GS(OFF)}$.

Solution: $g_m = g_{m_o} = \dfrac{-2I_{DSS}}{V_P} = \dfrac{-2I_{DSS}}{V_{GS(OFF)}}$

$$10\times10^{-3} = \frac{-2\times10\times10^{-6}}{V_{GS(OFF)}}$$

$$V_{GS(OFF)} = -2 \text{ mV}$$

Example 6: A FET has a drain current of 4 mA. If I_{DSS} = 6 mA and $V_{GS(OFF)} = -6$ V. Find the values of V_{GS} and V_p.

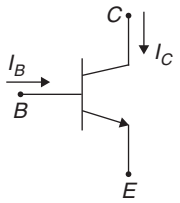
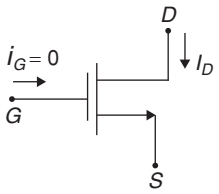
Solution: $I_D = 4$ mA; $I_{DSS} = 6$ mA

$$V_{GS} = V_{GS(OFF)}\left[1-\sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= -6\left[1-\sqrt{\frac{4\text{ mA}}{6\text{ mA}}}\right] = -1.1 \text{ V}$$

Pinch-off voltage, $V_p = V_{GS(OFF)} = -6$ V

Table 1 *Relation between BJT and JFET*

S. No.	BJT	JFET
i.		
ii.	$I_C = \beta \cdot I_B$	$I_D = I_{DSS}\left(1-\dfrac{V_{GS}}{V_P}\right)^2$
iii.	$I_C \approx I_E$	$I_D = I_S$
iv.	$V_{BE} = 0.7$ V	$I_G \approx 0$ A
v.	Current controlled (I_B) current device (I_C)	voltage controlled (V_{GS}) current device (I_D)

Comparisons of JFET and BJT

1. FET is a unipolar device i.e., operation depends only on the flow of majority carriers. BJT operations depends on both minority and majority charge carriers.
2. FET is a voltage controlled device and BJT is a current controlled device.
3. FET is less noisy than BJT (minority carriers more noise)
4. FET is smaller than the BJT's
5. BJT's are faster than the FET's.
6. The input circuit of FET is reverse biased. (i.e., input impedance higher $R_{in} \approx 100$ MΩ). FET offers a larger input impedance and lower output impedance. So FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input is forward biased.
7. FET does not suffer from minority charge carrier storage effects, it has 'higher switching speeds and cut-off frequency' BJT has lower switching speed and cut-off frequencies.
8. BJT's are cheaper than FET's.
9. FET amplifiers have low gain band width product due to the junction capacitance. (disadvantage)
10. FET has a negative (zero) temperature coefficient at high current levels, it prevents the FET thermal runaway. The BJT has a '+ve' temperature coefficient at high current levels which leads to thermal break down.
11. No current enters the gate of JFET i.e., $I_G = 0$ A. However, typical BJT base current I_B be a few μA.
12. In JFET, there are no junctions as in an ordinary transistor. The conduction is through an *n*-type or *p*-type semiconductor material.

Example 7: A JFET has I_{DSS} = 16 mA and $V_P = -4$ V. $V_{GS} = -2$ V, the value of drain current is

(A) 8 mA. (B) 4 mA.
(C) 16 mA. (D) 6 mA.

Solution: (B)

We know, $I_D = I_{DSS}\left[1-\dfrac{V_{GS}}{V_P}\right]^2$

$$= 16\left[1-\frac{(-2)}{(-4)}\right]^2 \times 10^{-3}$$

$$= 16 \times 10^{-3} \times 0.25 = 4 \text{ mA}.$$

Example 8: The transconductance of a JFET used as a voltage amplifier is 2500 $\mu\Omega^{-1}$ and drain resistance is 15 kΩ. The voltage gain of the amplifier is

(A) 25 (B) 30
(C) 37.5 (D) 40

Solution: (C)

Given $g_m = 2500 \times 10^{-6}\Omega^{-1}$

$R_D = 15 \times 10^3\Omega$

voltage gain $A_V = g_m \cdot R_D$

$= 2500 \times 10^{-6} \times 15 \times 10^3$

$= 37.5.$

Example 9: In a *p*-channel JFET, the charge carriers are

(A) Electrons. (B) Holes.
(C) Both electrons and holes. (D) Either e^-'s or holes.

Solution: (B)

Example 10: If the reverse bias voltage is increased, then the width of the conducting channel of JFET is

(A) Increased. (B) Decreased.
(C) Remains same. (D) None of the above

Solution: (B)

Example 11: The input control parameter of JFET is

(A) Source voltage. (B) Gate voltage.
(C) Drain voltage. (D) None of these

Solution: (B)

Example 12: The gate voltage in a JFET at which drain current becomes zero is called
(A) Break down (B) Active.
(C) Cut-off. (D) Saturation.

Solution: (C)

Example 13: In a common source JFET amplifier, the output voltage is
(A) In phase with the input. (B) 90° out of phase.
(C) 180°out of phase with input. (D) None of the above.

Solution: (C)

Example 14: The constant current region of a JFET lies between
(A) Cut-off and saturation.
(B) Cut-off and pinch off.
(C) Pinch off and break down regions.
(D) 0 and I_{DSS}.

Solution: (C)

Example 15: The trans-conductance of a JFET ranges from
(A) 0.5 to 30 mA/V. (B) 100 to 500 mA/V.
(C) 500 to 750 mA/V. (D) Above 750 mA/V.

Solution: (A)

Introduction to MOSFET

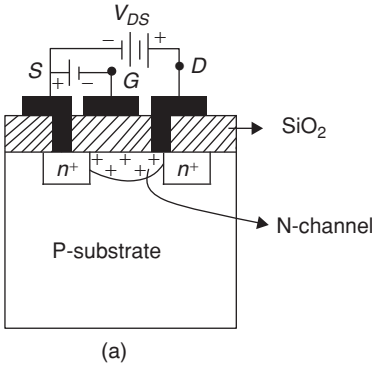
The main drawback of JFET is that its gate must be reverse biased for proper operations of the device i.e., it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. The name MOSFET stands for "Metal Oxide Semiconductor Field Effect Transistor". The insulating layer between the gate and the channel has resulted in another name for the device, insulated gate FET or IGFET.

MOSFET's broadly classified into two categories. These are

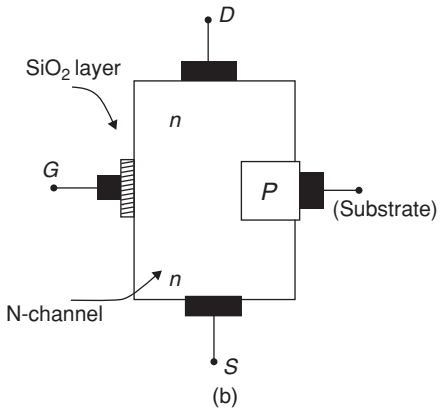
1. Depletion mode MOSFET or D-MOSFET
2. Enhancement mode MOSFET or E-MOSFET

D-MOSFET

Construction of the n-channel depletion mode MOSFET



(a)



(b)

Figure 6 (a) *N*-Channel, (b) D-MOSFET

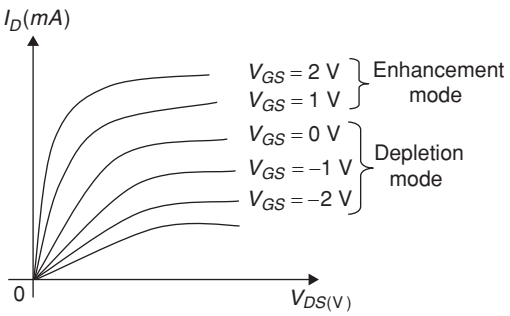
The D-MOSFET can be operated in both the depletion-mode and the enhancement-mode. The device consists of a *p*-type substrate into which are diffused two heavily doped n^+-type semiconductor blocks. In between the blocks, is a lightly doped *n*-type channel. The majority carriers e^-'s flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region.

A thin layer of metal oxide (SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. A SiO_2 is an insulator; therefore gate is insulated from the channel. Since the gate is insulated from the channel, we can apply either negative (or) positive voltage to the gate. Since, D-MOSFET can be operated in both depletion-mode and enhancement-mode JFET can be operated only In depletion-mode. If a '+ve' potential is applied to the drain, since electrons of the *n*-type drain block are attracted towards the +ve terminal. If a '–ve' voltage is applied to the gate, +ve charge carriers would be induced in the *n*-type channel. There tend to join with free e^-'s present in the channel, they creating a depletion region and increasing the channel resistance the MOSFET is termed as depletion mode MOSFET.

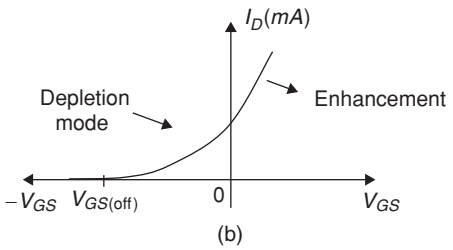
If the gate is given +ve bias with respective source, the number of charge carriers i.e., e^-'s in the *n*-channel further increases, with the result that the drain current increases. It means that a '+ve' gate bias the depletion mode MOSFET can be operated as enhancement mode MOSFET shown in Figure 6.

Transfer characteristics of D-MOSFET

The drain and transfer characteristics of a *n*-channel depletion–enhancement mode MOSFET.



(a)



Fifure 7 (a) Drain characteristic, (b) transfer characteristics

Enhancement Mode MOSFET or E-MOSFET

There are two types, enhancement *p*-channel and *n*-channel types.

p-channel E-MOSFET

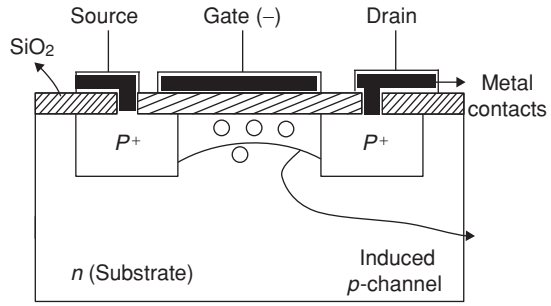


Figure 8 *p*-channel Enhancement type

A lightly doped *n*-type substrate into which two highly doped p^+ regions are diffused. The p^+ regions act as source and drain. A thin layer of SiO_2 is grown over the surface of the structure, and holes are cut into the oxide layer, allowing contact with the source and drain. The gate metal area is overlaid on the oxide, covering the entire channel region. Metal contacts are made to the drain and source. When the gate is given negative supply voltage, positive charges will be induced is the substrate between the source and drain, forms an inversion layer. Current flows from source to drain through the channel.

n-Channel E-MOSFET

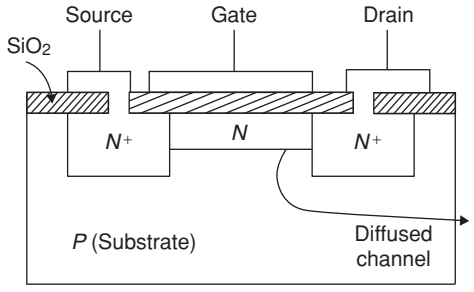


Figure 9 *n*-channel E-MOSFET

A *n*-channel is diffused between two *n*+ regions is a *p*-substrate. With gate potential is zero, maximum drain current flows. When gate is given negative supply, positive ions are induced into the channel, thus reduces the conductivity. The operation is similar to that of JFET.

$$I_D = I_{DSS} = \left(1 - \frac{V_{DS}}{V_T}\right)^2 \text{ for } |V_{DS}| \geq |V_T|$$

E-MOSFET operates only in the enhancement mode and has no depletion mode, and the E-MOSFET has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer. The minimum value of V_{GS} of proper polarity that turn 'ON' the E-MOSFET is called 'Threshold voltage' [$V_{GS(Th)}$]. The *n*-channel device requires positive $V_{GS} \geq V_{GS(th)}$ and the *p*-channel device requires negative $V_{GS} (\geq V_{GS(th)})$.

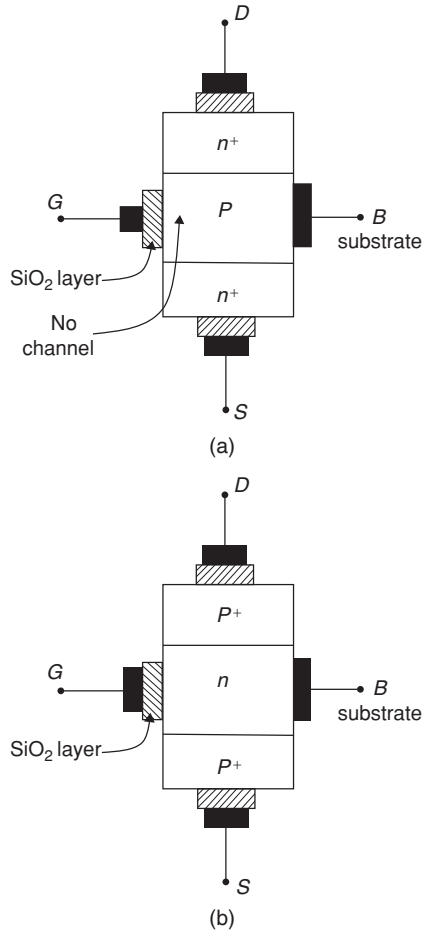


Figure 10 (a) *n*-channel E-MOSFET, (b) *p*-channel E-MOSFET

It does not conduct when gate-source voltage $V_{GS} = 0$. This is also called normally-off MOSFET. In these MOSFETs drain current I_D flows only when $V_{GS} \geq V_{GS(th)}$.

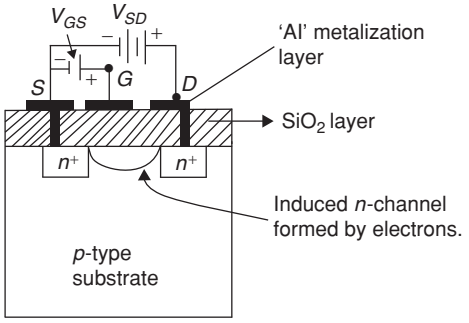


Figure 11 Operation of *n*-channel E MOSFET

Case (1): $V_{GS} = 0$ V and V_{DS} = +ve voltage

When V_{DS} = +ve voltage and no potential is applied to the gate, the two *n*-regions and one *p*-substrate form two *p*-n junctions connected back-back with a resistance of the *p*-substrate. Both the junctions are in reverse biased at the same time. So only a reverse leakage current flows.

The minimum value of gate-to-source voltage V_{GS} that is required to form the inversion layer (*N*-type) is termed the gate-to-source threshold voltage $V_{GS(th)}$.

If $V_{GS} < V_{GS(th)}$ then $I_D = 0$ A (OFF)

$V_{GS} \geq V_{GS(th)}$ (ON)

An *n*-type inversion layer connects the source to drain and the drain current I_D is large depending upon the device being used $V_{GS(th)}$ may vary from less than 1 V to more than 5 V.

JFET and D-MOSFET are classified as the depletion mode devices because their conductivity depends on the action of depletion layers. E-MOSFET is classified as an enhancement mode device because its conductivity depends on the action of the inversion layer. Depletion mode devices are normally ON when $V_{GS} = 0$ V also. Whereas enhancement-mode devices are normally OFF when $V_{GS} = 0$ V shown in Figure 12.

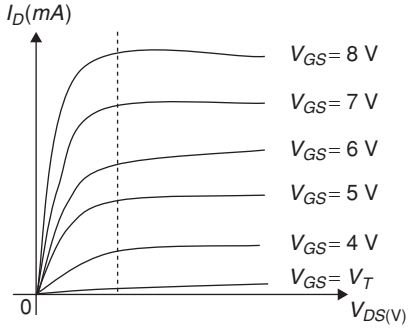


Figure 12 Drain characteristic of an *n*-channel enhancement MOSFET

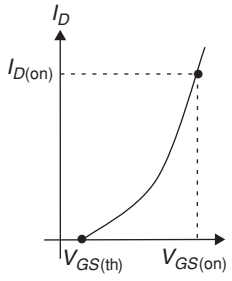


Figure 13 Transconductance curve for *n*-channel E-MOSFET

Drain current relations

$$I_D = K[V_{GS} - V_T]^2$$

Where, $V_T = V_{GS(th)}$ = Threshold voltage

$$K = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2}$$

Increasing order of input impedance:

BJT < op-amp < JFET < MOSFET

Relationship between I_D and V_{GS}

MOSFET in triode region

$$V_{GS} \geq V_{th}$$

$$I_D = \mu_n C_{ox} \cdot \frac{W}{L}\left[[V_{GS} - V_T] \cdot V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Where, $K'_n = \mu_n C_{ox}$

$\Rightarrow$ transconductance parameter

$\frac{W}{L}$ $\Rightarrow$Aspect ratio

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\therefore I_D = K_n' \frac{W}{L}\left[(V_{GS} - V_T) \cdot V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = K\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Where, $K = \frac{\mu_n C_{ox} W}{L}$

Case (2): MOSFET in saturation region

$V_{GS} \geq V_T$ and $V_{DS} \geq (V_{GS} - V_T)$

Let $V_{DS(sat)} = V_{GS} - V_T$

$$\therefore \quad I_D = \frac{K_n'}{2}\frac{W}{L}[(V_{GS} - V_T)^2] = K(V_{GS} - V_T)^2$$

Where, $K = \frac{\mu_n C_{ox} W}{2L}$

For *n*-channel E-MOSFET

The Body Effect

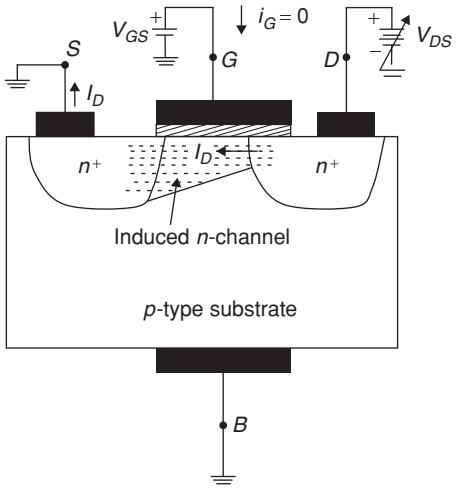


Figure 14 Enhancement *n*-MOS transistor as V_{DS} is increased.

In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the p-n junction between the substrate and the induced channel having a constant zero (cut-off) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether shown in Figure 14.

In Integrated circuits, the substrate is usually common to many MOS transistors.

In order to maintain the cut off condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply. In an N-MOS circuit, (the most positive in a P-MOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in an n-channel) will have an effect on device operation.

The reverse bias voltage will widen the depletion region; this in turn reduces the channel depth. To return the channel to its former state V_{GS} has to be increased the effect of V_{SB} on the channel can be represented as a change in the V_T.

$$V_T = V_{TO} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$$

Where,

$V_{T0} \Rightarrow$ Threshold voltage for $V_{SB} = 0$;

$\varphi_f \Rightarrow$ constant ($2\varphi_f \approx 0.6$ V)

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}}$$

$V_T \rightarrow$ Threshold voltage

From the above equation it indicates that an incremental change in V_{SB} gives rise to an incremental change in V_T i.e., in an incremental change in I_D even through V_{GS} = constant.

Since the body voltage controls I_D, then the body acts as another gate for the MOSFET, this is known as the body effect.

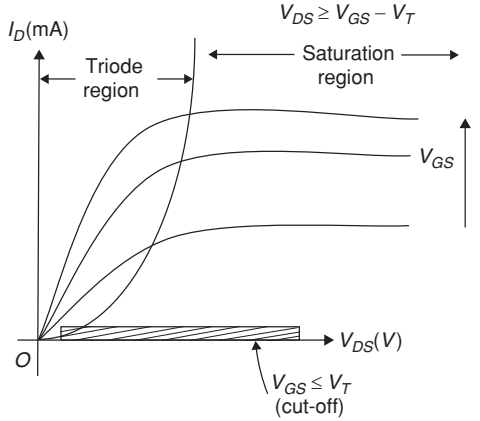
Note: Both V_T and K are temperature sensitive the magnitude V_T decreases by about 2 mV/°C rise in temperature and K' decrease with temperature.

$\therefore V_T \downarrow \Rightarrow I_D \uparrow K' \downarrow \downarrow$ (more decrement)

$\Rightarrow$ i.e., $I_D \downarrow$ (Overall effect)

$\therefore$ The overall observed effect of a temperature increases in a decrease in drain current.

Summary of the MOSFET Current – Voltage Characteristics



N-MOS Transistor

1. Triode region: conditions.

   $V_{GS} \geq V_T$ (MOSFET ON)

   $V_{DS} < V_{GS} - V_T$ (continuous channel)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

I-V relationships

$$I_D = \mu_n \cdot C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

For $V_{DS} << 2(V_{GS} - V_T)$

$$\therefore r_{ds} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\left[\mu_n C_{ox} \cdot \frac{W}{L}(V_{GS} - V_T)\right]}$$

2. Operation in the saturation region: conditions.

   $V_{GS} \geq V_T$, $V_{DS} \geq V_{GS} - V_T$

   $\therefore V_{DS(sat)} = V_{GS} - V_T$

I-V relationships

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

If $\lambda = 0$

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox} \cdot \frac{W}{L}(V_{GS} - V_T)^2$$

Threshold voltage:

$$V_T = V_{TO} + \gamma(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f})$$

Parameters

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \text{ (F/m}^2\text{)}$$

$$K'_n = \mu_n C_{ox} \text{ (A/V}^2\text{)}$$

$$\gamma = \frac{1}{V_A} (V^{-1})$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{OX}(V^{1/2})}$$

Constants

$$\varepsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$$

$$\varepsilon_{ox} = 3.9\varepsilon_0$$

$$\varepsilon_s = 11.7\varepsilon_0$$

$$Q = 1.6 \times 10^{-19} \text{ C}$$

PMOS Transistors

Conditions for triode region

$V_{GS} \leq V_T$ (ON State)

$V_{DS} \geq V_{GS} - V_T$ (continuous channel)

$$I_D = K'_p \frac{W}{L}\left[(V_{GS} - V_T)\cdot V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$K'_p = \mu_P C_{ox}.$$

Conditions for saturation region

$V_{DS} \le V_{GS} - V_t$ (pinched-off channel)

$$I_D = \frac{1}{2}\cdot K'_P \frac{W}{L}[V_{GS} - V_T]^2(1 + \lambda \cdot V_{DS})$$

Where V_{GS}, V_T, λ and V_{DS} all are negative.
If $\lambda = 0$

$$I_D = \frac{1}{2}\mu_P \cdot C_{ox} \cdot \frac{W}{L}[V_{SG} - |V_T|]^2$$

Example 16: The threshold voltage of an *n*-channel MOSFET can be increased by
(A) Increasing the channel dopant concentration.
(B) Reducing channel dopant concentration.
(C) Reducing the gate-oxide-thickness.
(D) Reducing the channel length.

Solution: (C)

Example 17: A MOS capacitor made using *p*-type substrate is in the accumulation mode. The dominant charge in the channel is due to the presence of
(A) Holes. (B) Electrons.
(C) Positively charged ions. (D) Negatively charged ions.

Solution: (A)

Example 18: The drain of an *n*-channel MOSFET is shorted to the gate so that $V_{GS} = V_{DS}$. The threshold voltage (V_T) of MOSFET is 2 V. If the drain current I_D is 2.5 mA for $V_{GS} = 3$ V then for $V_{GS} = 5$ V I_D is
(A) 4 mA. (B) 9 mA.
(C) 15 mA. (D) 22.5 mA.

Solution: (D)
If $V_{GS} = V_{DS} \Rightarrow$ MOSFET in saturation region,

$$\therefore \quad I_D = \frac{k_n}{2}(V_{GS} - V_T)^2$$

$$I_D = 2.5 \text{ mA}$$

$$V_{GS} = 3 \text{ V}; \; V_T = 2 \text{ V}$$

$$2.5\times10^{-3} = \frac{k_n}{2}(3-2)^2$$

$$K_n = 5 \times 10^{-3} \text{ A/V}^2$$

$$K_n = 5 \text{ mA/V}^2$$

$$\therefore \quad I_D = \frac{K_n}{2}(V_{GS} - V_T)^2$$

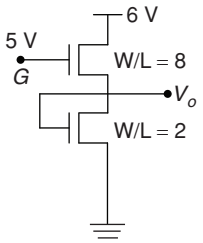
$V_{GS} = 5$ V then,

$$I_D = 2.5 \times 10^{-3}(5-2)^2$$

$$I_D = 22.5 \text{ mA}.$$

Example 19: In the circuit shown below for the MOS transistors. $\mu_n C_{ox}$ = 150 μA/V², and the threshold voltage V_T = 1 V. The voltage V_0 at the source of the upper transistor is
(A) 2 V. (B) 3 V.
(C) 4 V. (D) 5 V.

Solution: (B)



From the figure,

$$I_{DS_1} = I_{DS_2}$$

$$\therefore \quad \frac{K_{n_1}}{2}(V_{GS1} - V_T)^2 = \frac{K_{n_2}}{2}(V_{GS2} - V_T)^2$$

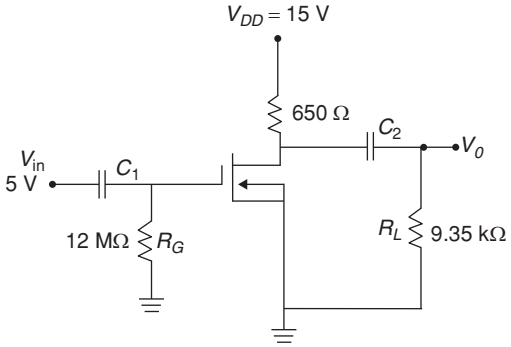
Where $V_{GS_1} = 5 - V_0$

$$\frac{1}{2}(150\times10^{-6})(8)(5 - V_o - 1)^2 = \frac{1}{2}\cdot(150\times10^{-6})(2)(V_0 - 1)^2$$

$$2(5 - V_o - 1) = (V_o - 1) \Rightarrow 8 - 2\,V_0 = V_o - 1$$

$$3\,V_o = 9 \Rightarrow V_o = 3 \text{ V}.$$

Common Data for Questions 20 and 21: The D-MOSFET used in the amplifier shown below, has an I_{DSS} = 10 mA and g_m = 3.5 mA/V



Example 20: The DC drain-to-source voltage V_{DS} is
(A) 5 V. (B) 7.5 V.
(C) 8.5 V. (D) 10 V.

Solution: (C)
The input signal is capacitive coupled to the gate.
For D.C value of $V_{GS} = 0$ V (C → open ciruit)

$$\therefore \; I_D = I_{DSS} = 10 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D \cdot R_D$$

$$= 15 - 10 \times 10^{-3} \times 650 = 8.5 \text{ V}.$$

Example 21: The AC output voltage for V_{in} = 450 mA is
(A) 0.96 V. (B) 1.2 V.
(C) 1.5 V. (D) None of the above

Solution: (A)

$$R_{AC} = R_D \| R_L$$

$$= 650\ \Omega \| 9.35\ \text{k}\Omega$$

$$= \frac{6.077\times10^{6}}{10\times10^{3}}$$
$$= 608\ \Omega$$
$$V_{out} = A_v \cdot V_{in} = (g_m \cdot R_{AC}) \cdot V_{in}$$
$$= 3.5\times10^{-3}\times608\times450\times10^{-3}$$
$$= 0.96\ \text{V}.$$

Example 22: The MOSFET differs from a JFET mainly because
(A) The JFET has a pn junction.
(B) The MOSFET has two gates.
(C) Of power rating.
(D) None of the above

Solution: (A)

Example 23: The *p*-channel D-MOSFET with a negative V_{GS} is operating in
(A) The depletion mode. (B) The enhancement-mode.
(C) Cut-off region. (D) Saturation region.

Solution: (B)

Common Data for Questions 24 and 25: Consider a process technology for which $L_{min} = 0.5\ \mu m$, $t_{ox} = 10$ nm, $\mu_n = 500\ cm^2/V\text{-sec}$, and $V_T = 0.7$ V.

Example 24: Find C_{ox} and K_n
(A) $3.45\times10^{-3}\ F/m^2$, $172.5\ mA/V^2$
(B) $5.5\times10^{-3}\ F/m^2$, $172.5\ \mu A/V^2$
(C) $3.45\times10^{-3}\ F/m^2$, $172.5\ \mu A/V^2$
(D) $3.45\times10^{-6}\ F/m^2$, $172.5\ mA/V^2$

Solution: (C)

We know $C_{ox} = \frac{\varepsilon_{0x}}{t_{0x}} = \frac{3.95\cdot\varepsilon_0}{t_{0x}}$

$$= \frac{3.45\times10^{-11}}{10\times10^{-9}} = 3.45\times10^{-3}\ F/m^2.$$

$$K_n = \mu_n \cdot C_{ox}$$
$$= 500\times\frac{cm^2}{V-s}\times3.45\times10^{-3}\ F/m^2$$
$$= 500\times10^{-4}\ \frac{m^2}{V-sec}\times3.45\times10^{-3}\ F/m^2$$
$$= 500\times3.45\times10^{-7}\ A/V^2$$
$$K_n = 172.5\ \mu A/V^2.$$

Example 25: For a MOSFET with $\frac{W}{L} = 5$, calculate the values of V_{GS} and $V_{DS(min)}$ to operate the transistor in the saturation region with a DC current $I_D = 80\ \mu A$
(A) $V_{GS} = 1.13$, $V_{DS} = 0.43$ V
(B) $V_{GS} = 0.43$ V, $V_{DS} = 1.13$ V
(C) $V_{GS} = 2.25$ V, $V_{DS} = 1.55$ V
(D) None of the above

Solution: (A)

We know $I_D = \frac{K_n}{2}\cdot\frac{W}{L}(V_{GS}-V_T)^2$

$I_D = 80\ \mu A$

$$80\times10^{-6} = \frac{172.5}{2}\times10^{-6}\times5(V_{GS}-V_T)^2$$
$$(V_{GS}-V_T)^2 = 0.1855$$
$$V_{GS}-V_T = V_{DS(min)} = 0.43\ \text{V}$$
$$V_{GS} = 0.43 + 0.7 = 1.13\ \text{V}.$$

Example 26: The value of V_{GS} required causing the device to operate as a 1.25 kΩ resistor for very small V_{DS} is
(A) $V_{GS} = 1.2$ V (B) $V_{GS} = 1.8$ V
(C) $V_{GS} = 1.63$ V (D) $V_{GS} = 2$ V

Solution: (C)
For the MOSFET in the triode region V_{DS} very small

$$I_D = K_n \cdot \frac{W}{L}(V_{GS}-V_T)V_{DS}\left(\text{neglect}\ \frac{1}{2}V^2{}_{DS}\right)$$

We know $r_{DS} = \frac{V_{DS}}{i_D}$, small V_{DS}

$$r_{DS} = \frac{1}{K_n\left(\frac{W}{L}\right)(V_{GS}-V_T)}$$
$$1250 = \frac{1}{172.5\times10^{-6}(V_{GS}-V_T)\times5}$$
$$V_{GS}-V_T = 0.9275$$
$$V_{GS} = 1.63\ \text{V}.$$

Example 27: An *n*-channel JFET has $I_{DSS} = 1$ mA and $V_p = -4$ V. Its transconductance g_m (mA/V) for an applied gate to source voltage V_{GS} of –3 V is

Solution: $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1-\frac{V_{GS}}{V_P}\right)$

$$= \frac{2\times1\times10^{-3}}{4}\left(1-\frac{-3}{-4}\right)$$
$$= \frac{2\times1\times10^{-3}}{4\times4} = 0.125\ \text{mA/V}.$$

Example 28: An ideal *p*-channel MOSFET has $C_{ox} = 8\times10^{-8}\ F/cm^2$. $\mu_p = 300\ cm^2/Vs$, $l = 2\ \mu m$, $t_{ox} = 250\ A°$, $V_{TP} = -0.8$ V, $w = 15\ \mu m$. If transistor is operating in non saturation region at $V_{SD} = 0.6$ V, value of g_m is

Solution: $I_D = \frac{\mu C_{ox} w}{2L}\left(2(V_{GS}+V_T)V_{SD} - V_{SD}^2\right)$

$$I_D = \frac{300\times8\times10^{-8}\times15\times10^{-4}}{2\times2\times10^{-4}}\left[2(V_{SG}+V_T)V_{SD} - V_{SD}^2\right]$$
$$= 9\times10^{-5}\left[2(V_{SG}+V_T)V_{SD} - V_{SD}^2\right]$$
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 9\times10^{-5}\times2\times V_{SD}$$
$$= 0.6\times9\times10^{-5}\times2 = 0.108\ \text{ms}.$$

Example 29: For a given JFET, $I_{DSS} = 15$ mA, $V_P = -4$ V, $V_{DS} = 10$ V. Value of resistance R_S for a drain current of $I_{DS} = 7$ mA is

Solution: $I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$

$$7\times10^{-3} = 15\times10^{-3}\left(1-\frac{(V_{GS})}{-4}\right)^2$$

$$0.6831 = 1-\frac{V_{GS}}{-4}$$

$$V_{GS} = 0.3168\times 4$$

$$= -1.2674$$

$$V_{GS} = -I_{DS}\cdot R_s$$

$$R_s = \frac{1.2674}{7\text{ mA}}$$

$$= 181.05\ \Omega.$$

Example 30: A JFET fixed bias configuration has an operating point defined by $V_{GSQ} = -2$ V and $I_{DQ} = 5.625$ mA with $I_{DSS} = 10$ mA and $V_P = -8$ V. $Y_{os} = 40$ µs. Determine the value of *Av* and *rd*.

Solution: $g_m = \frac{2I_{DSS}}{|V_p|} = \frac{2\times10\text{ mA}}{8\text{ V}} = 2.5$ ms

$$g_m = g_{m_o}\left(1-\frac{V_{gsQ}}{V_p}\right) = 2.5\text{ ms}$$

$$\left(1-\frac{-2}{-8}\right) = 1.88\text{ ms}$$

$$A_v = -g_m R_D = -1.88\text{ ms}\times 2\text{ k}\Omega = -3.76$$

$$R_d = \frac{1}{y_o} = \frac{1}{40\,\mu\text{s}} = 25\text{ k}\Omega.$$

Example 31: Consider an *n*-channel depletion mode MOSFET having the parameters $V_{TN} = -1.5$ V and $K_n = 1$ mA/V^2. If $V_{GS} = 0$ V and $V_{DS} = 0.3$ V then I_D is

Solution: $V_{DS(\text{sat})} = V_{GS} - V_{TN}$

$$= 0 - (-1.5) = 1.5\text{ V}.$$

$$V_{DS} < V_{DS(\text{sat})}$$

Biased in non-saturated region

$$I_D = kn\left[2(V_{GS}-V_{TN})V_{DS} - V_{DS}^2\right]$$

$$= 1[2(0-1.5)0.3-(0.3)^2]$$

$$= 1[2(1.5)0.3-(0.3)^2]$$

$$= [0.9-0.09] = 0.81\text{ mA}.$$

Common Data for Questions 32 and 33: Consider an *n*-channel Si JFET with the parameters $N_a = 5\times10^{15}$/cm^3, $N_d = 10^{18}$/cm^3. $a = 0.3$ µm, $L = 6$ µm, $w = 25$ µm, $\mu_n = 1000$ cm^2/VS. $V_{GS} = 0$

Example 32: The pinch off current I_{D1} is

Solution: $I_{D1} = \frac{\mu(eN_a)^2 wa^3}{6\varepsilon L}$

$$= \frac{1000\times(0.6\times10^{-19}\times5\times10^{15})^2\times25\times10^{-4}\times(0.3\times10^{-4})^3}{6\times(11.7\times8.85\times10^{-14}\times6\times10^{-4})}$$

$$= \frac{1000\times6.4\times10^{-7}\times 6.75\times10^{-17}}{3727.62\times10^{-18}}$$

$$= \frac{4.32\times10^{-20}}{3727.62\times10^{-18}} = 1.15\times10^{-5} = 0.015\text{ mA}.$$

Example 33: Maximum drain current $I_{DI(\text{sat})}$ is

Solution: $I_{D_1}(\max) = I_{D_1}\left[1-\frac{3Vbi}{Vpo}\left(1-\frac{2}{3}\sqrt{\frac{Vbi}{Vpo}}\right)\right]$

$$V_{po} = \frac{ea^2Na}{2\varepsilon_o}$$

$$= \frac{(1.6\times10^{-19})(5\times10^{15})\times(3\times10^{-4})^2}{2(11.7\times8.85\times10^{-14})}$$

$$= 0.347\text{ V}$$

$$V_{bi} = 0.0259\ln\left(\frac{(5\times10^{15}\times10^{18})}{(1.5\times10^{10})^2}\right)$$

$$= 0.0259\ln\left(\frac{5\times10^{33}}{2.25\times10^{20}}\right)$$

$$= 0.0259\ln(2.22\times10^{13}) = 0.79593\text{ V}$$

$$I_{Di\max} = 0.15\left(1-\left(3\times\frac{0.795}{0.347}\right)\right)\left(1-\frac{2}{3}\sqrt{\frac{0.796}{0.347}}\right]$$

$$= 3.2\text{ mA}.$$

Common Data for Questions 34 and 35: An *n*-channel JFET has a pinch of voltage of −3.5 V and $I_{DSS} = 6$ mA.

Example 34: At what value of V_{GS} will I_{DS} equal to 2 mA?

Solution: $I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$

$$V_{GS} = -3.5\left(1-\sqrt{\frac{2\times10^{-3}}{6\times10^{-3}}}\right)$$

$$= -3.5\ (0.42264)$$

$$= -1.4792\text{ V}.$$

Example 35: Find the value of g_m at this I_{DSS}?

Solution: $g_m = \frac{-2I_{DSS}}{V_P}\times\left(1-\frac{V_{GS}}{V_P}\right)$

$$g_m = \frac{-2\times6\times10^{-3}}{-3.5}\left(1-\frac{1.4772}{3.5}\right]$$

$$= \frac{-2\times6\times10^{-3}\times0.57737}{-3.5}$$

$$= 1.97\text{ ms}.$$

EXERCISES

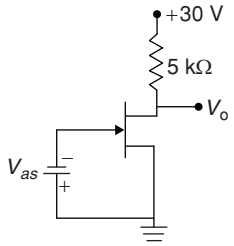
Practice Problems I

Directions for questions 1 to 27: Select the correct alternative from the given choices.

1. Find the resistivity of a *p*-channel Ge JFET with half channel height of 2 μm and pinch-off voltage of 3.94 V. (Consider $\mu_p = 1800$ cm²/V-sec. $\varepsilon_r = 16$)

(A) 0.02 Ω-cm (B) 0.2 Ω-cm
(C) 0.02 Ω-m (D) 0.2 Ω-m

2.



For the given *n*-channel JFET, $I_{Dss} = 6$ mA and $I_D = 2.5$ mA when $V_{GS} = -1$ V.

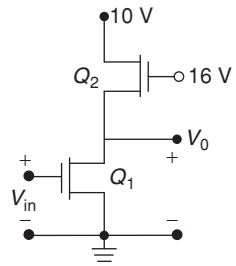
Calculate V_{GS} for a drain current of 3 mA is

(A) −0.71 V (B) −0.79 V
(C) −0.86 V (D) −0.69 V

3. Consider an *n*-channel silicon JFET with $a = 4$ μm, $W = 120$ μm and $L = 6$ μm. Find drain to source resistance for $V_{GS} = 0$ V if channel resistivity is 10 cm.

(A) 425 Ω (B) 625
(C) 475 (D) 675

4.



Assume threshold voltage of both transistors is 2 V and $\beta_1 = \beta_2$. Find V_o when $V_{in} = 6$ V.

(A) 5 V (B) 13.25 V
(C) 8.35 V (D) 3.25 V

5. Consider a MOSFET with $V_T = 0.7$ V, W = 8 μm, $L = 0.8$ μm, $K = 194$ μA/v².

The value of $V_{DS_{min}}$ need to operate the transistor in saturation region with a D.C current $I_D = 100$ μA.

(A) 1.02 V (B) 0.7 V
(C) 0.32 V (D) 1.72 V

6. Consider a MOSFET with $V_T = 0.7$ V, $W = 8$ μm, $L = 0.8$ μm, $K = 194$ μA/v².

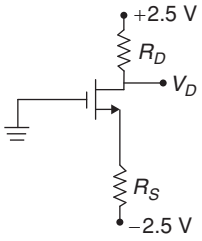
The value of V_{Gs} required causing the device to operate as a 100 resistor for very small V_{DS}.

(A) 1.02 V (B) 1.2 V
(C) 0.52 V (D) 1.52 V

7. An *n*-MOS enhancement transistor with $V_T = 0.7$ V conducts a current of $I_D = 100$ μA when $V_{GS} = V_{DS} = 1.2$ V. Find the value of I_D for $V_{Gs} = 1.5$ V and $V_{DS} = 3$ V.

(A) 128 μA (B) 100 μA
(C) 256 μA (D) 200 μA

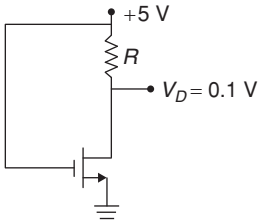
8.



Assume $V_T = 1$ V, $K = 60$ μA/V² and $\frac{W}{L} = \frac{120}{3}$. Find the value of R_S and R_D so that the transistor operates at $I_D = 0.3$ mA and $V_D = 0.4$ V.

(A) 7 k and 3.3 k
(B) 3.3 k and 7 k
(C) 5 k and 3.3 k
(D) 3.3 k and 5 k

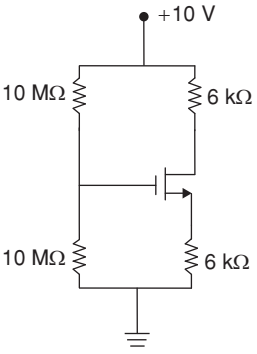
9.



Assume $V_T = 1$ V and $K \cdot \frac{W}{L} = 1$ mA/V². Find the value of *R*, to obtain a drain voltage of 0.1 V

(A) 11.4 k (B) 12.4 k
(C) 10.5 k (D) 9.6 k

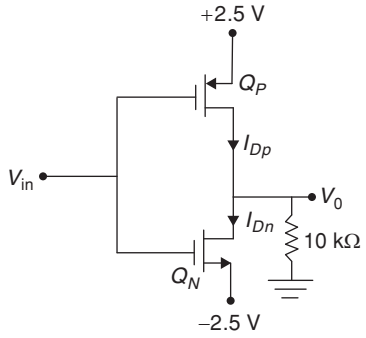
10.



Let $V_T = 1$ V, $K \cdot \frac{W}{L} = 1$ mA/V^2. Find the region of operation and drain current.

(A) Active, 0.89 mA (B) Saturation, 0.89 mA
(C) Active, 0.5 mA (D) Saturation, 0.5 mA

11.

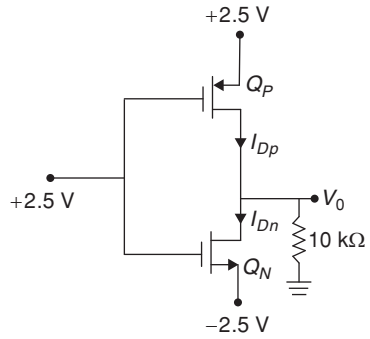


Assume both *n*-MOS and *p*-MOS has same $K \cdot \frac{W}{L} = 1$ mA/V^2 and $V_{t_n} = -V_{t_p} = 1$ V.

Find I_{DN} and I_{DP}, when $V_{in} = 0$ V

(A) 1.125 mA, 0 mA
(B) 0 mA, 1.125 mA
(C) 1.125 mA, 1.125 mA
(D) 0 mA, 0 mA

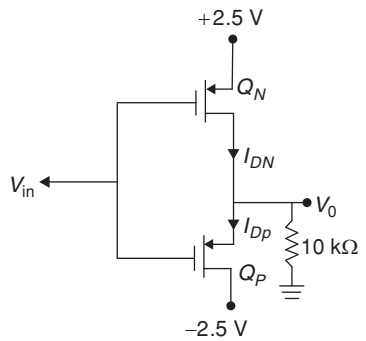
12.



Assume $V_T = 1$ V $K \cdot \frac{W}{L} = 1$ mA/V^2 for both. Find V_o when $V_{in} = +2.5$ V.

(A) –2.44 V (B) +2.44 V
(C) 5 V (D) 0 V

13.

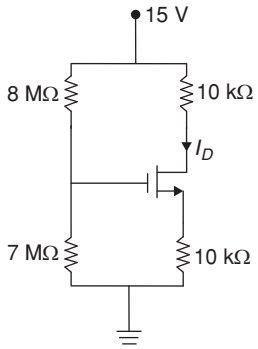


Assume both transistors are perfectly matched with $K \cdot \frac{W}{L} = 1$ mA/V^2 and $V_{t_n} = -V_{t_p} = 1$ V.

Find V_o when $V_{in} = +2.5$ V.

(A) –1.04 V (B) +1.04 V
(C) 0 V (D) +2.5 V

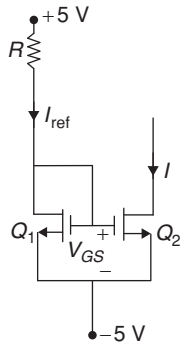
14.



Assume the MOSFET has V_T = 1 V and $K \cdot \frac{W}{L}$ = 1 mAV^2. If the current flowing is $I_D = 0.5$ mA initially, calculate the percent change in the value of I_D when the MOSFET is replaced with another having same $K \cdot \frac{W}{L}$ but $V_T = 1.5$ V.

(A) Decreases by 9% (B) Increases by 9%
(C) Remains same (D) None of the above

15.



Assume $V_T = 1$ V, $K \cdot \left(\frac{W}{L}\right)_1$, = 0.8 mA/V^2 and two Transistors Q_1 and Q_2 having equal length but widths related by $W_2 = 5W_1$. Find the value of *R*, to obtain *I* = 0.5 mA.

(A) 45 kΩ (B) 85 kΩ
(C) 65 kΩ (D) 55 kΩ

16. For a CMOS inverter with matched MOSFETS having $V_{t_n} = -V_{t_p} = 1$ V and $V_{DD} = 5$ V.

Find noise margin for HIGH level.

(A) 2.1 V
(B) 2.5 V
(C) 2.9 V
(D) 2 V

17. For a CMOS inverter with matched MOSFETS having $V_{t_n} = -V_{t_p} = 1$ V and $V_{DD} = 5$ V

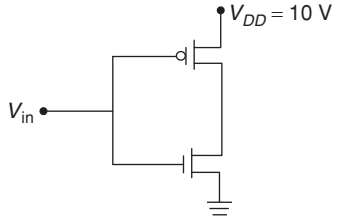
Find noise margin for LOW level.

(A) 2.1 V
(B) 2.9 V
(C) 2.5 V
(D) 2 V

18. A 1.2 μm CMOS inverter uses $L_n = L_p = 1.2$ μm, $W_n = 1.8$ μm, $k_n = 80$ μA/V², $k_p = 27$ μA/v², $V_{t_n} = 0.8$ V, $V_{DD} = 5$ V. Calculate the value of output resistance of the inverter when $V_o = V_{oL}$.

(A) 1 k (B) 1.5 k
(C) 2 k (D) 3 k

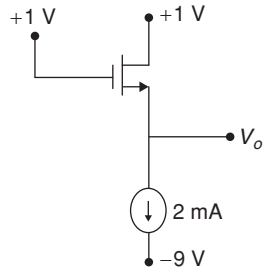
19.



Assume $V_{t_n} = -V_{t_p} = 2$ V, $\left(\frac{W}{L}\right)_n = 20$, $\left(\frac{W}{L}\right)_p = 40$ and $\mu_n C_{ox} = 2\mu_p$, $C_{ox} = 20$ μA/v². Find the peak current drawn from V_{DD} during switching.

(A) 1.2 mA
(B) 1.8 m A
(C) 0.8 mA
(D) 1.6 Ma

20.



Assume $V_t = +1$ V, $K \cdot \left(\frac{W}{L}\right) = 1$ mA/V². Find V_o for the circuit shown.

(A) +2 V (B) −2 V
(C) −9 V (D) +1 V

Common Data for Questions 21 and 22: For a depletion mode NMOS transistor with $V_t = -2$ V and $K\left(\frac{W}{L}\right) = 2$ mA/V².

21. Find the minimum V_{DS} required to operate in the saturation region when $V_{gs} = +1$ V

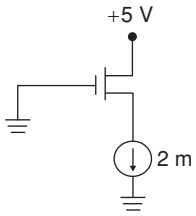
(A) −1 V (B) +1 V
(C) 2 V (D) 3 V

22. For a depletion mode NMOS transistor with $V_t = -2$ V and $K\left(\frac{W}{L}\right) = 2$ mA/V².

The value of drain current I_D, when $V_{gs} = +1$ V is _____

(A) 3 mA (B) 6 mA
(C) 7.5 mA (D) 9 mA

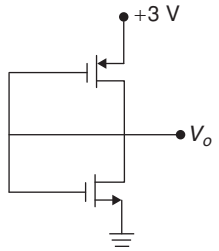
23.



For the depletion mode MOSFET, assume $K\left(\frac{W}{L}\right) = 4$ mA/V² and $V_t = -2$ V. Find the voltage across the source terminal.

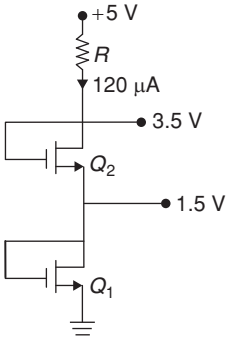
(A) −1 V (B) +1 V
(C) −3 V (D) +3 V

24. Assume $k_P = 2.5$ μA/V², $k_n = 10$ μA/V², $|V_t| = 1$ V, $L = 10$ μm, $W = 30$ μm. Find the output voltage V_o as shown.



(A) 4.1 V (B) 2.0 V
(C) 2.8 V (D) 4.2 V

25.

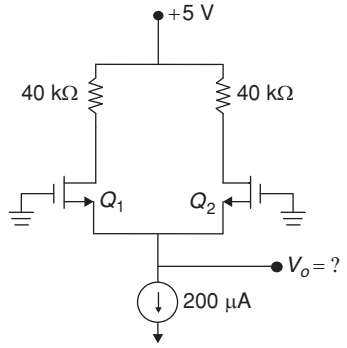


Assume each NMOS transistor has $V_t = 1$ V, $K = 120$ μA/V², $L_1 = L_2 = 1$ μm.

Find the value of gate width of Q_2.

(A) 8 μm (B) 4 μm
(C) 2 μm (D) 1 μm

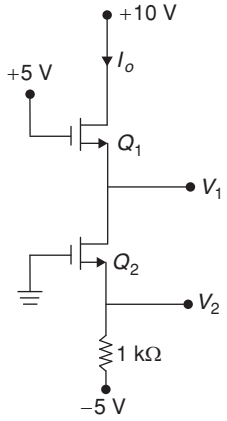
26.



Assume both Transistors have $V_t = 1$ V, $K = 100\ \mu A/V^2$, $\frac{W}{L} = 20$. Find the value of V_o indicated.

(A) 1.32 V
(B) 1.68 V
(C) −1.32 V
(D) −1.68 V

27. Assume each transistor has $V_t = 1$ V, and $K \cdot \frac{W}{L} = 2$ mA/V^2. Find the current flowing through drain of Q_1.



(A) 1.23 mA
(B) 2.44 mA
(C) 1.48 mA
(D) 2.65 mA

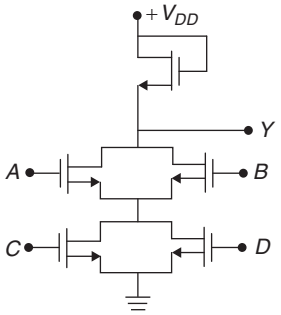
Practice Problems 2

Directions for questions 1 to 18: Select the correct alternative from the given choices.

1. Find the pinch off voltage of a silicon *n*-channel JFET with half channel height of 2 μm and donor concentration of 7×10^{14} atoms/cm^3

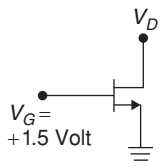
(A) 3.1 V
(B) 4.1 V
(C) 2.1 V
(D) 1.1 V

2. The logic function realized by the given circuit is _____



(A) $\overline{(A+C)(B+D)}$
(B) $\overline{(A+C)}+\overline{(B+D)}$
(C) $\overline{(A+B)}+\overline{(C+D)}$
(D) $\overline{A+B+C+D}$

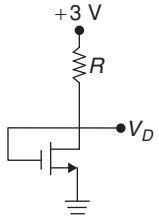
3.



For the given NMOS enhancement with $K = 100\ \mu A/v^2$, $W = 10$ μm, $L = 1$ μm and $V_T = 0.7$ V. Find the region of operation and drain current when $V_D = 0.9$ V.

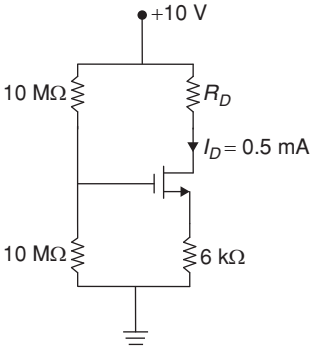
(A) Triode region, 275 μA
(B) Saturation, 320 μA
(C) Triode, 320 μA
(D) Saturation, 275 μA

4. Find the value of aspect ratio (W/L) and R, to obtain drain current of 160 μA and V_{DS} of 1 V.
Assume $V_T = 0.6$ V
$K = 200\ \mu A/V^2$



(A) 8 and 25 k
(B) 10 and 25 k
(C) 10 and 12.5 k
(D) 8 and 12.5 k

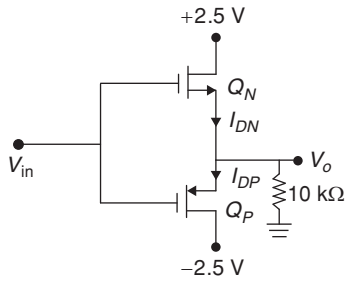
5.



Let $V_T = 1$ V and $K \cdot \frac{W}{L} = \frac{1\ mA}{V^2}$. Find the largest value that R_D can have, while the transistor remains in saturation with 0.5 mA of drain current.

(A) 8 k
(B) 10 k
(C) 12 k
(D) 16 k

6.

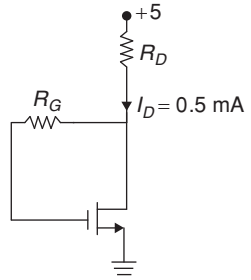


Assume both transistors are perfectly matched with $K \cdot \frac{W}{L} = 1 \text{ mA/V}^2$ and $V_{t_n} = V_{t_p} = 1 \text{ V}$

Find I_{D_N} and I_{D_P}, when $V_{\text{in}} = 0$ V.

(A) 0 mA, 0 mA (B) 0 mA, 0.104 mA
(C) 0.104 mA, 0 mA (D) 0.104 mA, 0.104 mA

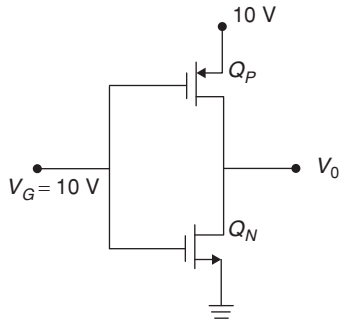
7.



Assume $V_T = 1 \text{ V}, K \cdot \frac{W}{L} = 1 \text{ mA/v}^2$. Find the value of R_D.

(A) 3 k (B) 6 k
(C) 9 k (D) 7.5 k

8.



The given CMOS inverter has $V_{t_n} = -V_{t_p} = 2 \text{ V}, \left(\frac{W}{L}\right)_p = 40, \left(\frac{W}{L}\right)_n = 20,$ $\mu_n C_{ox} = 20 \ \mu \text{ A/V}^2$.

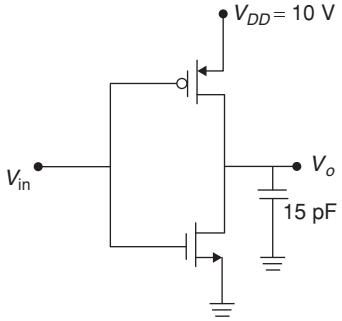
Find the maximum current that the inverter can sink while $V_O = 0.5$ V.

(A) 0 mA (B) 1.25 mA
(C) 1.55 mA (D) 1.75 mA

9. A 1.2 µm CMOS inverter uses $L_p = L_n = 1.2$ µm, $W_N = 1.8$ µm. Find the value of W_p that would result in Q_N and Q_P being matched. Assume $K_n = 80$ µA/V², $K_P = 27$ µA/V², $V_{t_n} = 0.8$ V and $V_{DD} = 5$ V.

(A) 1.8 µm (B) 3.6 µm
(C) 5.4 µm (D) 7.2 µm

Common Data for Questions 10 and 11:



Assume $V_{t_n} = -V_{t_p} = 2$ V, $\left(\frac{W}{L}\right)_n = 20; \left(\frac{W}{L}\right)_p = 40, K_n = 2k_p = 20 \ \mu\text{A/V}^2$.

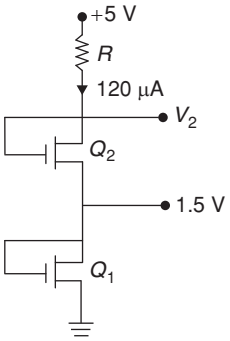
10. Find the dynamic power dissipation when the inverter is switched at a frequency of 2 MHz.

(A) 3 mW (B) 30 mW
(C) 6 mW (D) 15 mW

11. Average current drawn from the power supply is _____

(A) 0.3 mA (B) 0.6 mA
(C) 3 mA (D) 30 mA

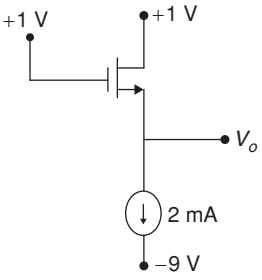
12.



Assume $V_t = 1$ V, $K = 120 \ \mu\text{A/V}^2$, $L_1 = L_2 = 1$ µm, $W_1 = 8$ µm, $W_2 = 2$ µm. Find the value of R indicated

(A) 25 k (B) 12.5 k
(C) 1.25 k (D) 2.5 k

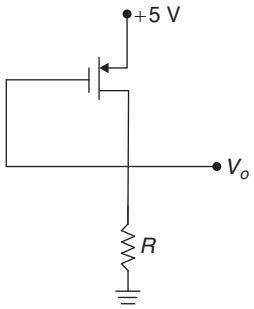
13.



Assume $V_t = +1$ V, $K \cdot \left(\frac{W}{L}\right) = 1 \text{ mA/V}^2$. Find V_o for the circuit shown.

(A) +2 V (B) −2 V
(C) −9 V (D) +1 V

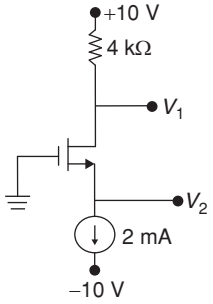
14.



For the PMOS transistor, assume V_t = –0.7 V, K_P = 60 μA/V², L = 0.8 μm. Find the value of W, in order to establish a drain current of 115 μA and a voltage, V_D of 3.5 V.

(A) 0.8 μm (B) 2.4 μm
(C) 4.8 μm (D) 3.6 μm

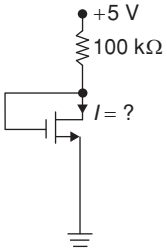
15. Assume $V_t = 2$ V, $K \cdot \frac{W}{L} = 1$ mA/V². Find V_1 and V_2 labeled as shown



(A) 2 V and 4 V (B) –2 V and –4 V
(C) 2 V and –4 V (D) –2 V and 4 V

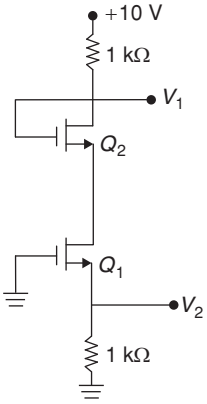
16. Assume $V_t = 1$ V, $K \cdot \left(\frac{W}{L}\right) = 0.4$ mA/V².

Find the value of drain current.



(A) 0.024 mA
(B) 0.036 mA
(C) 0.048 mA
(D) 0.072 mA

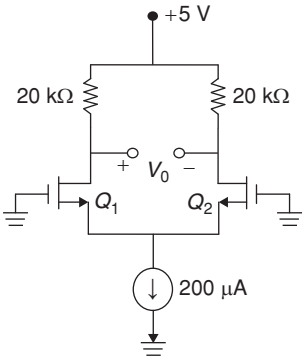
17.



Assume each NMOS has $V_t = 1$ V, and $K \cdot \frac{W}{L} = 2$ mA/V². Find the voltage V_1 shown in figure.

(A) 5.71 V
(B) 6.25 V
(C) 2.52 V
(D) 5.23 V

18.



Assume $V_t = 1$ Volt, $K = 100$ μA/V² and $W/L = 10$. Find the value of V_o as shown.

(A) 1 V (B) 3 V
(C) 2 V (D) 0 V

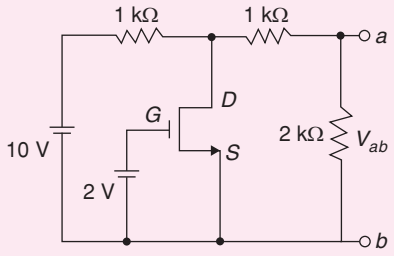
Previous Years' Questions

1. The value of R for which the PMOS transistor in figure will be biased in linear region is **[2004]**

(A) 220 Ω (B) 470 Ω
(C) 680 Ω (D) 1200 Ω

2. Assume that the n-channel MOSFET shown in figure is ideal, and that its threshold voltage is +1.0 V. The voltage V_{ab} between nodes a and b is:

[2005]

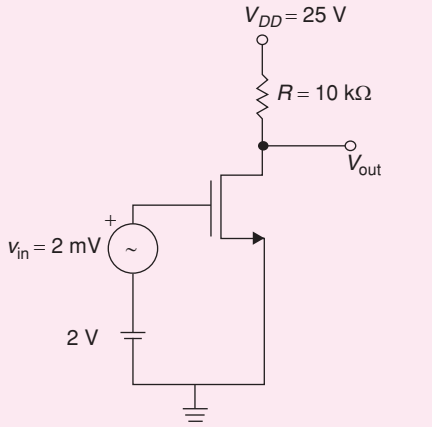


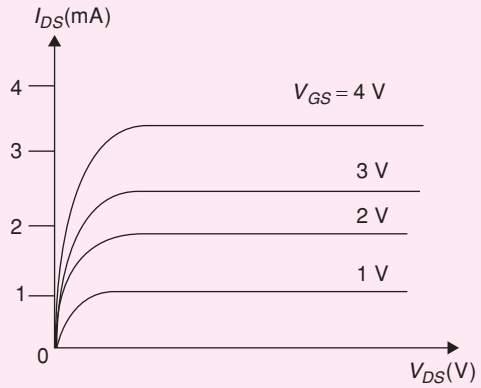
(A) 5 V (B) 2 V
(C) 1 V (D) 0 V

3. The conduction loss versus device current characteristic of a power MOSFET is best approximated by **[2005]**

(A) a parabola
(B) a straight line
(C) a rectangular hyperbola
(D) an exponentially decaying function

Common Data for Questions 4a and 4b: Assume that the threshold voltage fo the n-channel MOSFET shown in figure is +0.75 V. The output characteristics of the MOSFET are also shown. **[2005]**





4. (a) The transconductance of the MOSFET is:
(A) 0.75 ms (B) 1 ms
(C) 2 ms (D) 10 ms

(b) The voltage gain of the amplifier is:
(A) +5 (B) –7.5
(C) +10 (D) –10

Answer Keys

Exercises

Practice Problems 1

1. A	**2.** A	**3.** B	**4.** C	**5.** C	**6.** B	**7.** C	**8.** B	**9.** B	**10.** D
11. C	**12.** A	**13.** B	**14.** A	**15.** B	**16.** A	**17.** A	**18.** C	**19.** B	**20.** B
21. D	**22.** D	**23.** B	**24.** B	**25.** C	**26.** C	**27.** B			

Practice Problems 2

1. C	**2.** C	**3.** B	**4.** C	**5.** C	**6.** A	**7.** B	**8.** C	**9.** C	**10.** A
11. A	**12.** B	**13.** B	**14.** C	**15.** C	**16.** B	**17.** B	**18.** D		

Previous Years' Questions

1. D **2.** D **3.** A **4.** (a) B (b) D