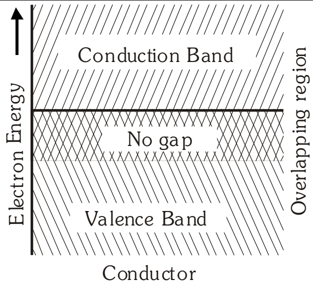
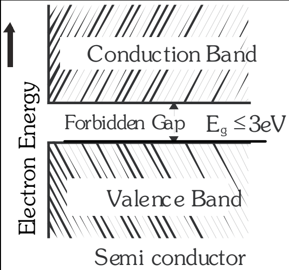
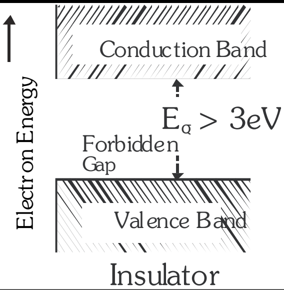
Semiconductor & Digital Electronics

Properties	Conductor	Semiconductor	Insulator
Resistivity	$10^{-2} - 10^{-8}\ \Omega m$	$10^{-5} - 10^{6}\ \Omega m$	$10^{11} - 10^{19}\ \Omega m$
Conductivity	$10^{2} - 10^{8}$ mho/m	$10^{-6} - 10^{5}$ mho/m	$10^{-19} - 10^{-11}$ mho/m
Temp. Coefficient of resistance (α)	Positive	Negative	Negative
Current	Due to free electrons	Due to electrons and holes	No current
Energy band diagram			
Forbidden energy gap	$\cong 0eV$	$\le 3eV$	$> 3eV$
Example	Pt, Al, Cu, Ag	Ge, Si, GaAs, GaF_2	Wood, plastic, Diamond, Mica

- **Number of electrons reaching from valence band to conduction band :** $n = AT^{3/2}e^{-\frac{\Delta Eg}{2kT}}$
- **CLASSIFICATION OF SEMICONDUCTORS :**

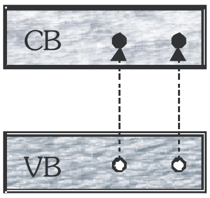
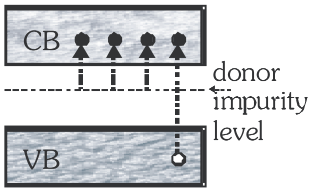
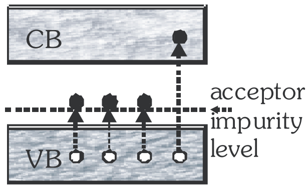
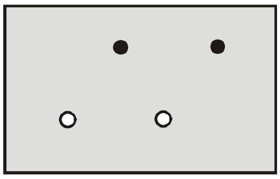
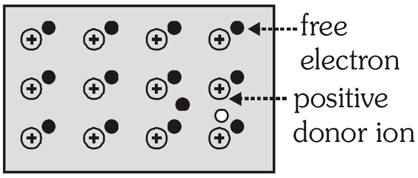
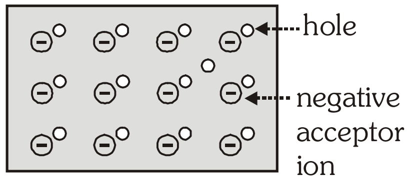
SEMICONDUCTOR

- Intrinsic semiconductor
  - (pure form of Ge, Si) $n_e = n_h = n_i$
- Extrinsic semiconductor (doped semicondutor)
  - N-type: pentavalent impurity (P, As, Sb etc.) donor impurity (N_D) $n_e >> n_h$
  - P-type: trivalent impurity (Ga, B, In, Al) acceptor impurity (N_A) $n_h >> n_e$

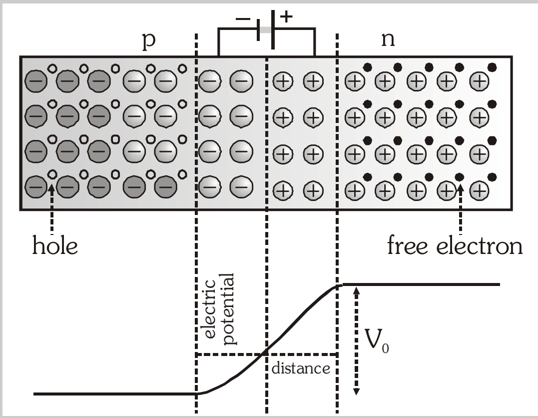
- **MASS-ACTION LAW** : $n_i^2 = n_e \times n_h$
  - ❐ For N-type semiconductor $n_e \simeq N_D$
  - ❐ For P-type semiconductor $n_h \simeq N_A$

CONDUCTION IN SEMICONDUCTOR

Intrinsic semiconductor	P - type	N - type
$n_e = n_h$	$n_h >> n_e$	$n_e >> n_h$
$J = ne\,[v_e + v_h]$ (Current density)	$J \cong e\,n_h\,v_h$	$J \cong e\,n_e\,v_e$
$\sigma = \frac{1}{\rho} = en\,[\mu_e + \mu_h]$ (Conductivity)	$\sigma = \frac{1}{\rho} \cong e\,n_h\,\mu_h$	$\sigma = \frac{1}{\rho} \cong e\,n_e\,\mu_e$

Intrinsic Semiconductor	N-type (Pentavalent impurity)	P-type (Trivalent impurity)
		
		
Current due to electron and hole	Mainly due to electrons	Mainly due to holes
$n_e = n_h = n_i$	$n_h << n_e$ ($N_D \approx n_e$)	$n_h >> n_e$ ($N_A \approx n_h$)
$I = I_e + I_h$	$I \approx I_e$	$I \approx I_h$
Entirely neutral	Entirely neutral	Entirely neutral
Quantity of electrons and holes are equal	Majority Electrons Minority Holes	Majority Holes Minority - Electrons

P-N JUNCTION
(At equilibrium condition)



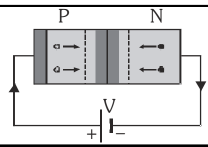
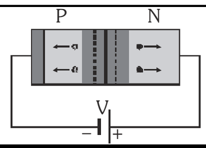
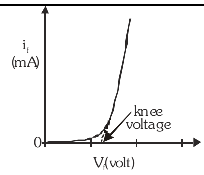
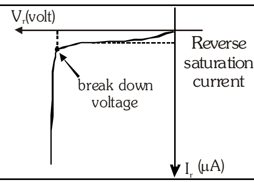
Direction of diffusion current : P to N side

and drift current : N to P side

If there is no biasing then diffusion current = drift current. So total current is zero

In junction N side is at high potential relative to the P side. This potential difference tends to prevent the movement of electron from the N region into the P region. This potential difference called a **barrier potential**.

COMPARISON BETWEEN FORWARD BIAS AND REVERSE BIAS

	Forward Bias		Reverse Bias
			
1	Potential Barrier reduces	1	Potential Barrier increases.
2	Width of depletion layer decreases	2	Width of depletion layer increases.
3	P-N jn. provide very small resistance	3	P-N jn. provide high resistance
4	Forward current flows in the circuit	4	Very small current flows.
5	Order of forward current is milli ampere.	5	Order of current is micro ampere for Ge or Nano ampere for Si.
6	Current flows mainly due to majority carriers.	6	Current flows mainly due to minority carriers.
7	Forward characteristic curves.	7	Reverse characteristic curve
			
8	Forward Resistance : $R_f = \frac{\Delta V_f}{\Delta I_f} \cong 100\Omega$	8	Reverse Resistance $: R_r = \frac{\Delta V_r}{\Delta I_r} \cong 10^6\Omega$
9	Order of knee or cut in voltage	9	Breakdown voltage
	Ge→ 0.3 V		Ge → 25 V
	Si → 0.7 V		Si → 35 V
	Special point : Generally $\frac{R_r}{R_f} = 10^3 : 1$ for Ge		$\frac{R_r}{R_f} = 10^4 : 1$ for Si

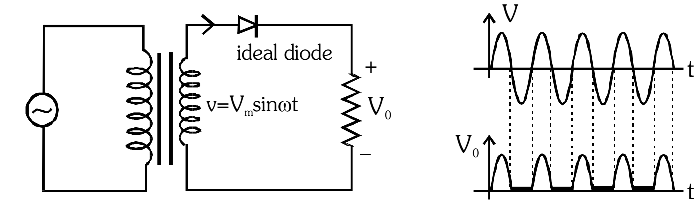
BREAKDOWN ARE OF TWO TYPES

Zener Break down	Avalanche Break down
Where covalent bonds of depletion layer, itself break, due to high electric field of very high Reverse bias voltage.	Here covalent bonds of depletion layers are broken by collision of "Minorities" which aquire high kinetic energy from high electric field of very-very high reverse bias voltage.
This phenomena take place in (i) P – N junction having "High doping" (ii) P – N junction having thin depletion layer Here P – N junction does not damage permanently "In D.C voltage stabilizer zener phenomena is used".	This phenomena takes place in (i) P – N junction having "Low doping" (ii) P – N junction having thick depletion layer Here P – N junction damages permanentaly due to abruptly increment of minorities during repeatative collisions.

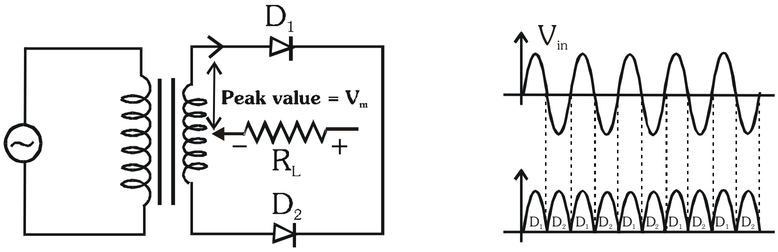
APPLICATION OF DIODE

- **Zener diode** : It is highly doped p-n junction diode used as a voltage regulator.
- **Photo diode** : A p-n junction diode use to detect light signals operated in reverse bias.
- **LED** : A p-n junction device that emits optical radiation under forward bias conditions
- **Solar cell** : Generates emf of its own due to the effect of sun radiations.

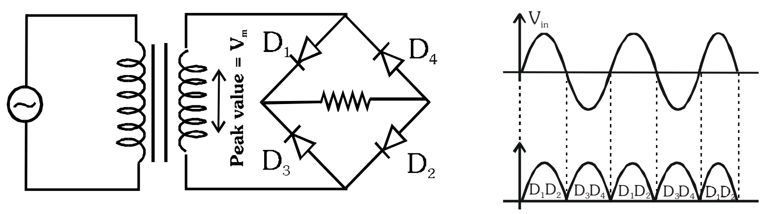
HALF WAVE RECTIFIER



CENTRE – TAP FULL WAVE RECTIFIER



FULL WAVE BRIDGE REACTIFIER



RIPPLE FACTOR : $r = \frac{I_{ac}}{I_{dc}}$

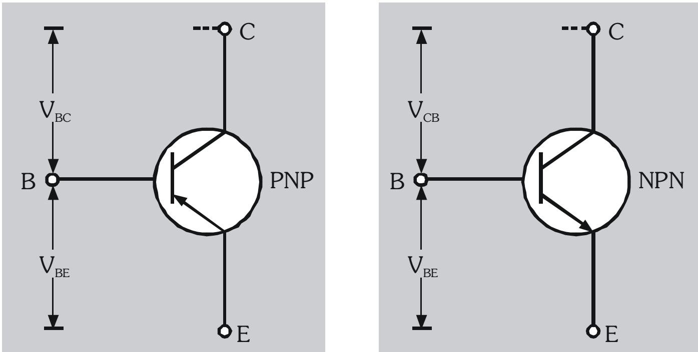
- For HWR $r = 1.21$
- For FWR $r = 0.48$

RECTIFIER EFFICIENCY: $\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_F + R_L)}$

For HWR : $\eta\% = \frac{40.6}{1 + \frac{R_F}{R_L}}$ & FWR $\eta\% = \frac{81.2}{1 + \frac{R_F}{R_L}}$

FOR TRANSISTOR

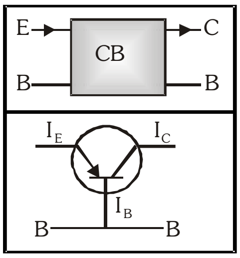
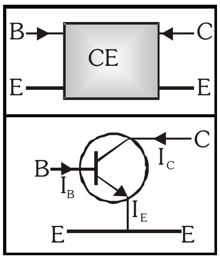
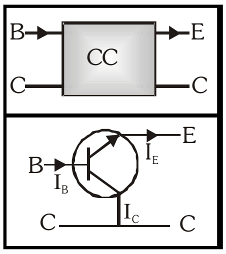
$$I_E = I_B + I_C$$



(a) (b)

COMPARATIVE STUDY OF TRANSISTOR CONFIGURATIONS

1. Common Base **(CB)** 2. Common Emitter **(CE)** 3. Common Collector **(CC)**

	CB	**CE**	**CC**
			
Input Resistance	Low (100 Ω)	High (750 Ω)	Very High ≅ 750 kΩ
Output resistance	Very High	High	Low
Current Gain	(A_I or α)	(A_I or β)	(A_I or γ)
	$\alpha = \frac{I_C}{I_E} < 1$	$\beta = \frac{I_C}{I_B} > 1$	$\gamma = \frac{I_E}{I_B} > 1$
Voltage Gain	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_E R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_C R_L}{I_B R_i}$	$A_V = \frac{V_o}{V_i} = \frac{I_E R_L}{I_B R_i}$
	$A_v = \alpha \frac{R_L}{R_i} \cong 150$	$A_v = \beta \frac{R_L}{R_i} \cong 500$	$A_v = \gamma \frac{R_L}{R_i} < 1$
Power Gain	$A_p = \frac{P_o}{P_i} = \alpha^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i} = \beta^2 \frac{R_L}{R_i}$	$A_p = \frac{P_o}{P_i} = \gamma^2 \frac{R_L}{R_i}$
Phase difference (between output and input)	same phase	opposite phase	same phase
Application	For High Frequency Amplifier	For Audible frequency Amplifier	For Impedance Matching

TRANSISTOR CHARACTERISTICS

- **Input resistance (r_1)** $\left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE=constant}}$

  (for CE)

- **Output resistance (r_0)** $\left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_{B=constant}}$

  (for CE)

- **Current amplification factor**

  - **For CE** $\beta_{ac} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE=constant}}$

  - **For CB** $\alpha_{ac} = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB=constant}}$

APPLICATIONS OF TRANSISTORS

There are three regions of transistor operation:

- **Cut off region** * **Active region** * **Saturation region**
- **Transistor as Voltage amplifier**

  * To operate it as an amplifer we need to fix its operating voltage somewhere in active region where it increases the strength of input ac signal and produces an amplified output signal.

  * Voltage gain $A_V = \frac{V_0}{V_i} = -\beta_{ac}\frac{R_{out}}{R_{in}}$

  * Power gain $A_P = A_V \times \beta_{ac}$

- **Transistor as a Switch**

  A transistor can be used as a switch if it is operated in its cutoff and saturation states only.

- **Transistor as an Oscillator**

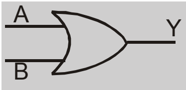
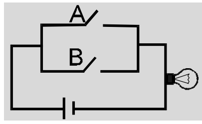
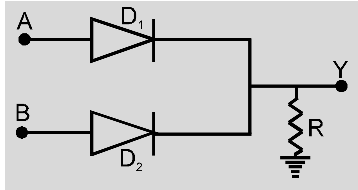
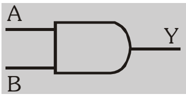
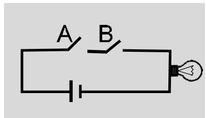
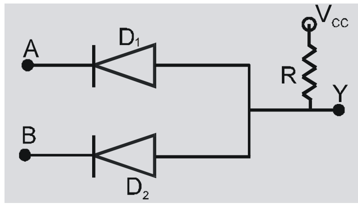
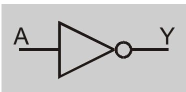
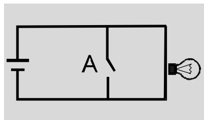
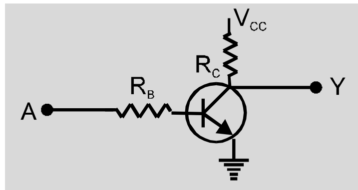
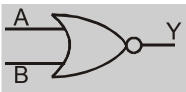
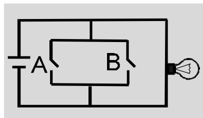
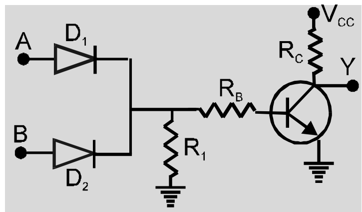
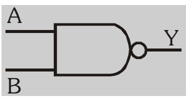
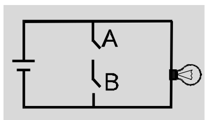
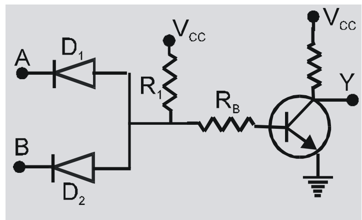
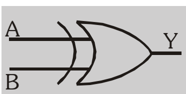
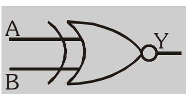
  An oscillator is a generator of an ac signal using positive feedback

  Frequency of oscillations if $f = \frac{1}{2\pi\sqrt{LC}}$

- **Relation between α, β and γ :**

$$\beta = \frac{\alpha}{1-\alpha},\ \gamma = 1+\beta,\ \gamma = \frac{1}{1-\alpha}$$

SUMMARY OF LOGIC GATES

Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)
OR		$Y = A + B$	A B Y 0 0 0 0 1 1 1 0 1 1 1 1		
AND		$Y = A.\ B$	A B Y 0 0 0 0 1 0 1 0 0 1 1 1		
NOT or Inverter		$Y = \overline{A}$	A Y 0 1 1 0		
NOR (OR +NOT)		$Y = \overline{A + B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 0		
NAND (AND+NOT)		$Y = \overline{A.B}$	A B Y 0 0 1 0 1 1 1 0 1 1 1 0		
XOR (Exclusive OR)		$Y = A \oplus B$ or $Y = \overline{A}.B + A\overline{B}$	A B Y 0 0 0 0 1 1 1 0 1 1 1 0		
XNOR (Exclusive NOR)		$Y = A \odot B$ or $Y = A.B + \overline{A}.\overline{B}$ or $Y = \overline{A \oplus B}$	A B Y 0 0 1 0 1 0 1 0 0 1 1 1		

DE MORGAN'S THEOREM

$$\overline{A + B} = \overline{A} \bullet \overline{B}, \quad \overline{A \bullet B} = \overline{A} + \overline{B}$$

OR	AND	NOT
$A + 0 = A$	$A.\ 0 = 0$	$A + \overline{A} = 1$
$A + 1 = 1$	$A.\ 1 = A$	$A \cdot \overline{A} = 0$
$A + A = A$	$A\ .\ A = A$	$\overline{\overline{A}} \cdot A = A$