

# 2

## Boolean Algebra, Logic Gates and K-Maps

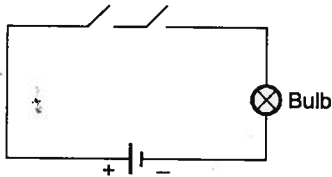


### Multiple Choice Questions

**Q.1** The precedence order while solving Boolean expression is

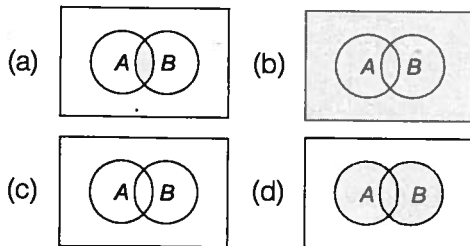
- (a)  $() < \text{OR} < \text{AND} < \text{NOT}$
- (b)  $() > \text{NOT} > \text{AND} > \text{OR}$
- (c)  $() < \text{NOT} < \text{AND} < \text{OR}$
- (d)  $() < \text{AND} > \text{NOT} > \text{OR}$

**Q.2** What logic gate is represented by the circuit shown below?



- (a) AND
- (b) NAND
- (c) NOR
- (d) EQUIVALENCE

**Q.3** The expression  $A + \bar{A}B$  is represented by



**Q.4** If  $X = 1$  in the logic equation

$$[X + Z\{\bar{Y} + (\bar{Z} + X\bar{Y})\}]\{\bar{X} + \bar{Z}(X + Y)\} = 1 \text{ then}$$

- (a)  $Y = Z$
- (b)  $Y = \bar{Z}$
- (c)  $Z = 0$
- (d)  $Z = 1$

[GATE-2009]

**Q.5** The Boolean expression

$$ABCD + A\bar{B}CD + ABC\bar{D} + A\bar{B}C\bar{D}$$

is equivalent to

- (a)  $A$
  - (b)  $AC$
  - (c)  $ABC$
  - (d)  $1$
- [ESE-2008]

**Q.6** If  $x$  and  $y$  are Boolean variables, which one of the following is the equivalent of  $x \oplus y \oplus xy$ ?

- (a)  $x + \bar{y}$
- (b)  $x + y$
- (c)  $0$
- (d)  $1$

[ESE-2004(EE)]

**Q.7** The Boolean expression  $\bar{Y}\bar{Z} + \bar{X}\bar{Y} + \bar{X}\bar{Z}$  is logically equivalent to

- (a)  $YZ + \bar{X}$
- (b)  $x\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z$
- (c)  $XYZ + \bar{X}\bar{Y}\bar{Z}$
- (d)  $XY + YZ + XZ$

**Q.8** The total number of Boolean functions that can be constructed for  $n$  Boolean variables is

- (a)  $n$
- (b)  $2^n$
- (c)  $(2^n)^n$
- (d)  $2^{2^n}$

[DRDO-2009]

**Q.9** With 4 Boolean variables, how many Boolean expressions can be formed?

- (a) 16
- (b) 256
- (c) 1024 (1 K)
- (d) 64 K ( $64 \times 1024$ )

[ESE-2002]

**Q.10** Consider the statement below:

1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.

2. If the output waveform from an OR gate is always HIGH, one of its input is being held permanently HIGH.

The statement, which is always true, is  
(a) Both 1 and 2 (b) Only 1  
(c) Only 2 (d) None of these

- Q.11** If the output of a logic gate is '1' when all its inputs are at logic '0', the gate is either  
(a) A NAND or A NOR  
(b) An AND or an EX-NOR  
(c) An OR or an NAND  
(d) An EX-OR or an EX-NOR [ESE-2014]

- Q.12** Which one of the following statements is correct?  
For a 4-input NOR gate, when only two inputs are to be used, the best option for the unused inputs is to  
(a) connect them to the ground  
(b) connect them to  $V_{CC}$   
(c) keep them open  
(d) connect them to the used inputs [ESE-2004(EE)]

- Q.13** How is inversion achieved using EX-OR gate?  
(a) Giving input signal to the two input lines of the gate tied together.  
(b) Giving input to one input line and logic zero to the other line.  
(c) Giving input to one input line and logic one to the other line.  
(d) Inversion cannot be achieved using EX-OR gate. [ESE-2002]

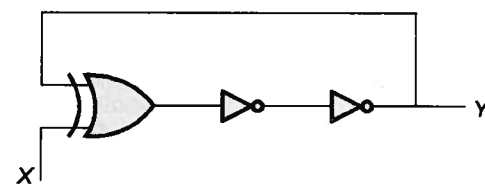
- Q.14** Consider:  
 $Y = A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A$  the  $Y$  is equivalent to:  
(a) 1 OR  $E$  (b) A EX OR 0  
(c) 1 NOR  $B$  (d) A AND A

- Q.15** The function  
 $f = (\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C) \oplus A$  can be written as:  
(a)  $B \oplus C$  (b)  $A \oplus B \oplus A$   
(c)  $A$  (d) None of these

- Q.16**  $[(A + \bar{A}\bar{B})(A + \bar{A}\bar{B})] + [(CD + \bar{C}\bar{D}) + (C \oplus D)] =$   
(a)  $B$  (b)  $A$   
(c) 0 (d) 1

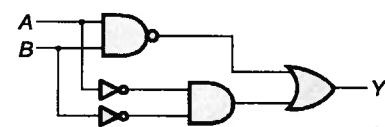
- Q.17** **Statement (I):** XOR gate is not a universal gate.  
**Statement (II):** It is not possible to realize any Boolean function using XOR gates only.  
(a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).  
(b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).  
(c) Statement (I) is true but Statement (II) is false.  
(d) Statement (I) is false but Statement (II) is true. [ESE-2012]

- Q.18** All the logic gates in the circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



- (a)  $X = 0$  (b)  $X = 1$   
(c)  $X = 0$  or 1 (d)  $X = Y$  [GATE-IN:2006]

- Q.19** The logic circuit of figure is a

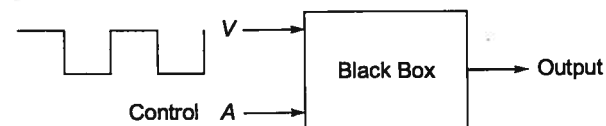


- (a) Half adder (b) XOR  
(c) Equality detector (d) NAND [GATE-2003]

- Q.20** If a variable is having Ex-OR operation itself 'n' number of times, then the result is  
(a) Complement of variable if 'n' is even.  
(b) Uncomplement of variable if 'n' is even.  
(c) Complement of the variable if 'n' is odd.  
(d) Uncomplement of the variable if 'n' is odd.

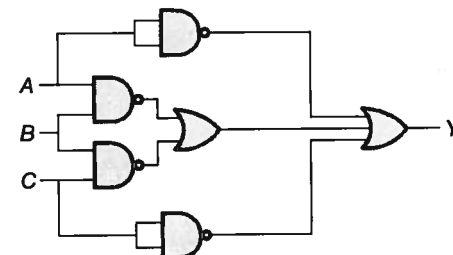
- Q.21** An odd function involving three Boolean variables is  
(a)  $\Sigma(1, 3, 5, 7)$  (b)  $\Sigma(0, 2, 4, 6)$   
(c)  $\Sigma(1, 2, 4, 7)$  (d)  $\Sigma(0, 3, 5, 6)$  [DRDO-2009]

- Q.22** Black box inverts the phase of input  $V$  when control 'A' is 1 and lets it pass through uninverted when control 'A' is 0 then circuit is



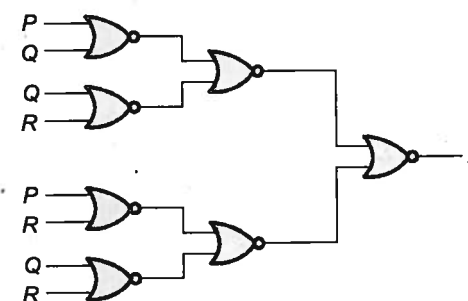
- (a) XNOR gate (b) XOR gate  
(c) NAND gate (d) NOR gate

- Q.23** For the logic circuit shown in figure below, the output 'Y' is equal to



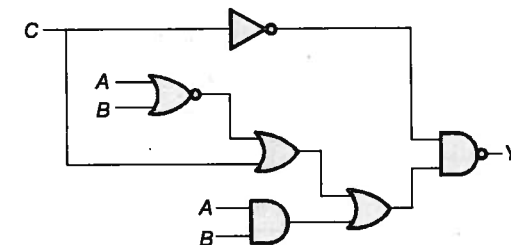
- (a)  $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{B} + \bar{C}$  (b)  $\bar{A}\bar{B} + \bar{B}\bar{C}$   
(c)  $\bar{A} + \bar{B} + \bar{C}$  (d) All of these

- Q.24** What is the boolean expression for the output  $f$  of the combinational logic circuit of NOR gates given below?



- (a)  $\bar{Q} + \bar{R}$  (b)  $\bar{P} + \bar{Q}$   
(c)  $\bar{P} + \bar{R}$  (d)  $\bar{P} + \bar{Q} + \bar{R}$  [GATE-2010]

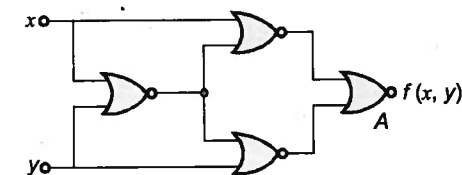
- Q.25** In the circuit shown in the figure, if  $C = 0$ , the expression for  $Y$  is



- (a)  $Y = \bar{A}\bar{B} + \bar{A}B$  (b)  $Y = A + B$   
(c)  $Y = \bar{A} + \bar{B}$  (d)  $Y = AB$

[GATE-2014]

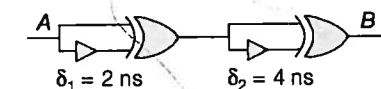
- Q.26** Identify the logic function performed by the circuit shown



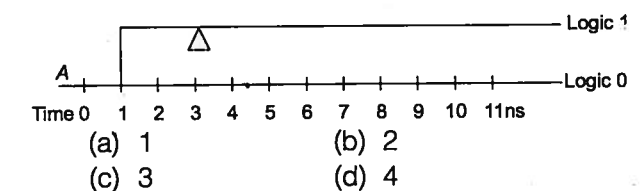
- (a) Exclusive OR (b) Exclusive NOR  
(c) NAND (d) NOR

[GATE-1993]

- Q.27** Consider the following circuit composed of XOR gates and non-inverting buffers.



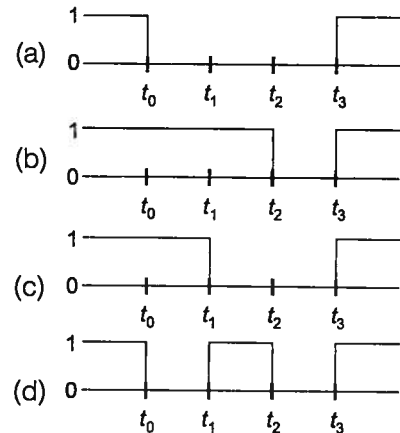
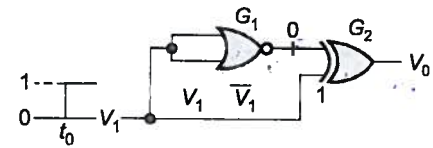
The non-inverting buffers have delays  $d_1 = 2$  ns and  $d_2 = 4$  ns as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns



[GATE-2003]

- Q.28** The gates  $G_1$  and  $G_2$  in the figure have propagation delays of 10 nsec and 20 nsec respectively. If the input  $V_i$  makes an abrupt

change from logic 0 to 1 at time  $t = t_0$ , then the output waveform  $V_0$  is  
 $(t_1 = t_0 + 10 \text{ ns}, t_2 = t_0 + 20 \text{ ns}, t_3 = t_0 + 30 \text{ ns})$



[GATE-2002]

Q.29 The switching expression corresponding to  $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$  is

- (a)  $BC'D' + A'C'D + AB'D$
- (b)  $ABC' + ACD + B'C'D$
- (c)  $ACD' + A'B'C' + AC'D'$
- (d)  $A'BD + ACD' + BCD'$

[ISRO-2009]

Q.30 The Boolean expression  $AC + B\bar{C}$  is equivalent to

- (a)  $\bar{A}C + B\bar{C} + AC$
- (b)  $\bar{B}C + AC + B\bar{C} + \bar{A}C\bar{B}$
- (c)  $AC + B\bar{C} + \bar{B}C + ABC$
- (d)  $ABC + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}C$

[GATE-EC:2004]

Q.31 What is the minimized logic expression corresponding to the given Karnaugh Map?

wx	yz			
	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

- (a)  $xz$
- (b)  $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}z + wxy$
- (c)  $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}z + wxy$
- (d)  $xz + \bar{w}yz + \bar{w}x\bar{y} + wxy + w\bar{y}z$

[ESE-2005]

Q.32 The function  $f(A, B, C, D) = \Sigma(5, 7, 9, 11, 13, 15)$  is independent of variable(s)

- (a)  $B$
- (b)  $C$
- (c)  $A$  and  $C$
- (d)  $D$

[DRDO-2009]

Q.33 Consider the following boolean function of four variables  
 $f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$ . The function is

- (a) independent of one variable
- (b) independent of two variables
- (c) independent of three variables
- (d) dependent on all the variables

[ISRO-2009]

Q.34 The min term of  $f(P, Q, R) = PQ + QR' + PR'$  is

- (a)  $m_2 + m_4 + m_6 + m_7$
- (b)  $m_0 + m_1 + m_3 + m_5$
- (c)  $m_0 + m_1 + m_6 + m_7$
- (d)  $m_2 + m_3 + m_4 + m_5$

[GATE-2010]

Q.35 The Boolean functions can be expressed in canonical SOP (sum of products) and POS (product of sums) form. For the functions,  $Y = A + \bar{B}C$ , which are such two forms

- (a)  $Y = \Sigma(1, 2, 6, 7)$  and  $Y = \Pi(0, 2, 4)$
- (b)  $Y = \Sigma(1, 4, 5, 6, 7)$  and  $Y = \Pi(0, 2, 3)$
- (c)  $Y = \Sigma(1, 2, 5, 6, 7)$  and  $Y = \Pi(0, 1, 3)$
- (d)  $Y = \Sigma(1, 2, 4, 5, 6, 7)$  and  $Y = \Pi(0, 2, 3, 4)$

[GATE-2008]

Q.36 The SOP (sum of products) form of a Boolean function is  $\Sigma(0, 1, 3, 7, 11)$ , where inputs are  $A, B, C, D$  ( $A$  is MSB, and  $D$  is LSB). The equivalent minimized expression of the function is

- (a)  $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{B})(\bar{C} + D)$

- (b)  $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + D)$
- (c)  $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + \bar{D})$
- (d)  $(\bar{B} + C)(A + \bar{B})(\bar{A} + \bar{B})(\bar{C} + D)$

[GATE-2014]

Q.37 What is the minimum number of NAND gates required to implement  $A + A\bar{B} + \bar{B}C(A + \bar{C})$ ?

- (a) 0
- (b) 2
- (c) 4
- (d) 6

[GATE-2004]

Linked Answer Questions (38 and 39):

The following Karnaugh map represents a function  $F$ .

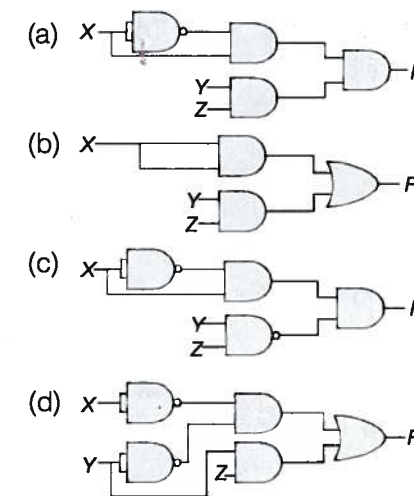
F	YZ			
	00	01	11	10
0	1	1	1	0
1	0	0	1	0

Q.38 A minimized form of the function  $F$

- (a)  $F = \bar{X}Y + YZ$
- (b)  $F = \bar{X} \cdot \bar{Y} + YZ$
- (c)  $F = \bar{X}\bar{Y} + YZ$
- (d)  $F = \bar{X}\bar{Y} + \bar{Y}Z$

[GATE-2010]

Q.39 Which of the following circuits is a realization of the above function  $F$ ?



[GATE-2010]

Q.40 The minterms for  $AB + ACD$  are

- (a)  $\bar{A}\bar{B}CD + A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}BCD$
- (b)  $AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD + A\bar{B}CD$
- (c)  $A\bar{B}CD + A\bar{B}C\bar{D} + ABC\bar{D} + \bar{A}BCD + A\bar{B}C\bar{D}$
- (d)  $AB\bar{C}\bar{D} + A\bar{B}CD + \bar{A}BCD + ABC\bar{D} + A\bar{B}C\bar{D}$

[ESE-2013]

Q.41 The minimized function  $f$  obtained from the K-map given below is

DE	BC		A'
	1		1
			1
			1
	1		1

- (a)  $C'E' + A'BCE + BCD'E$
- (b)  $B'C'E' + A'BCE + ABCD'E + BC'E$
- (c)  $C'E' + A'BCD + BCDE$
- (d)  $B'C'E + A'BCE + ABCD'E + BC'E$

[DRDO-2008]

Q.42 Which are the essential prime implicants of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

- (a)  $a'c$  and  $ac'$
- (b)  $a'c$  and  $b'c$
- (c)  $a'$  only
- (d)  $a'$  and  $bc'$

[GATE-2004]

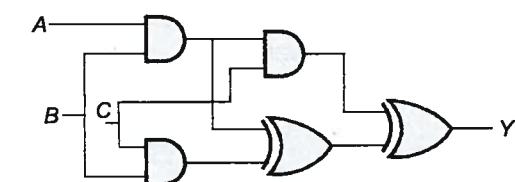
Q.43 Consider the Boolean function,

$$F(w, x, y, z) = wy + xy + \bar{w}xyz + \bar{w}\bar{x}y + xz + \bar{x}\bar{y}\bar{z}$$

Which one of the following is the complete set of essential prime implicants?

- (a)  $w, y, xz, \bar{x}\bar{z}$
- (b)  $w, y, xz$
- (c)  $y, \bar{x}\bar{y}\bar{z}$
- (d)  $y, xz, \bar{x}\bar{z}$

Q.44 The output of the combinational circuit given below is



- (a)  $A + B + C$
- (b)  $A(B + C)$
- (c)  $B(C + A)$
- (d)  $C(A + B)$

[GATE-2016]

Q.45 The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

- (a) 4
- (b) 5
- (c) 6
- (d) 7

[GATE-2016]

**Q.46** Following is the K-map of a Boolean function of five variables  $P, Q, R, S$  and  $X$ . The minimum sum-of-product (SOP) expression for the function is

PQ					PQ				
RS					RS				
00	0	0	0	0	00	0	1	1	0
01	1	0	0	1	01	0	0	0	0
11	1	0	0	1	11	0	0	0	0
10	0	0	0	0	10	0	1	1	0

$X=0$

$X=1$

- (a)  $\bar{P}\bar{Q}S\bar{X} + P\bar{Q}S\bar{X} + Q\bar{R}S\bar{X} + QR\bar{S}X$   
 (b)  $\bar{Q}S\bar{X} + Q\bar{S}X$  **(b)**  
 (c)  $\bar{Q}S\bar{X} + Q\bar{S}X$   
 (d)  $\bar{Q}S + Q\bar{S}$

[GATE-2016]

**Q.47** The chairman requested the aggrieved shareholders to \_\_\_\_\_ him.

- (a) bare with (b) bore with  
 (c) bear with (d) bare

[GATE-2016]

**Q.48** The Boolean expression  $\overline{(a+b+c+d)} + (b+\bar{c})$  simplifies is

- (a) 1 (b)  $\bar{a} \cdot \bar{b}$   
 (c)  $a, b$  (d) 0

[GATE-2016]

**Q.49** Consider the Boolean operator # with the following properties:

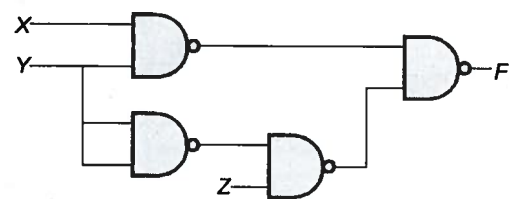
$$x \# 0 = x, x \# 1 = \bar{x}, x \# x = 0 \text{ and } x \# \bar{x} = 1.$$

Then  $x \# y$  is equivalent to

- (a)  $x\bar{y} + \bar{x}y$  (b)  $\bar{x}\bar{y} + \bar{x}\bar{y}$   
 (c)  $\bar{x}y + xy$  (d)  $xy + \bar{x}\bar{y}$

[GATE-2016]

**Q.50** In the digital circuit given below,  $F$  is:



- (a)  $XY + Y\bar{Z}$  (b)  $XY + \bar{Y}Z$   
 (c)  $\bar{X}\bar{Y} + Y\bar{Z}$  (d)  $XZ + \bar{Y}$

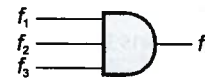
[GATE-2016]

## Numerical Data Type Questions

**Q.51** Consider the logical functions given below.

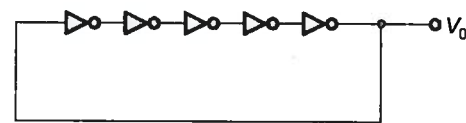
$$f_1(A, B, C) = \Sigma(2, 3, 4)$$

$$f_2(A, B, C) = \pi(0, 1, 3, 6, 7)$$

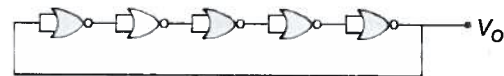


If  $f$  is logic zero, then maximum number of possible minterms in function  $f_3$  are \_\_\_\_\_.

**Q.52** For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency (in GHz) of the oscillator output?



**Q.53** The average propagation delay of each NOR gate shown below is 10 ns. The frequency of the output signal  $V_0$  is \_\_\_\_\_ MHz.



**Q.54** The minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate is \_\_\_\_\_.

[GATE-2004]

**Q.55** Minimum number of 2 input NAND gates required to implement the logic function  $F = A + B + C + D$  are \_\_\_\_\_.

**Q.56** The minimum number of 2 input NAND gates required to realize the Boolean function  $f(A, B, C) = A\bar{B}C$ .

**Q.57** Consider the function:

$$f = \bar{A}(\bar{B}C + BCD) + \bar{B}\bar{D}(A + C) + \bar{A}\bar{B}\bar{C}$$

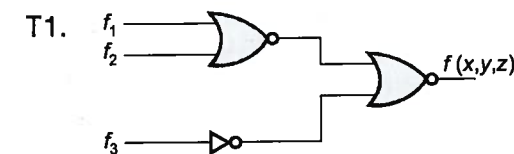
$$d = \bar{A}B(C\bar{D} + \bar{C}D) + ACD$$

Where ' $f$ ' represents Boolean function and ' $d$ ' represents don't care condition. Then simplified Boolean expression ' $f$ ' is reduced to \_\_\_\_\_ literals.

**Q.58** The number of prime-implicants for the given function  $f(A, B, C) = \Sigma m(0, 2, 5, 6, 7)$  is \_\_\_\_\_.

**Q.59** The number of essential prime-implicants in the given function  $f(w, x, y, z) = \Sigma m(0, 2, 6, 7, 8, 9, 13, 15)$  is \_\_\_\_\_.

## Try Yourself

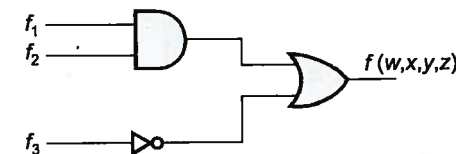


If  $f_1(x, y, z) = \Sigma m(0, 1, 3, 5)$ ,  
 $f_2(x, y, z) = \Sigma m(4, 5)$  and  
 $f(x, y, z) = \Sigma m(1, 4, 5)$   
 then  $f_3(x, y, z)$  is \_\_\_\_\_

- (a)  $\Sigma m(1, 4, 5)$   
 (b)  $\Pi M(1, 4, 5)$   
 (c)  $\Sigma m(1, 4, 5) + d(2, 6, 7)$   
 (d)  $\Pi M(1, 4, 5) \cdot d(2, 6, 7)$

[Ans: (c)]

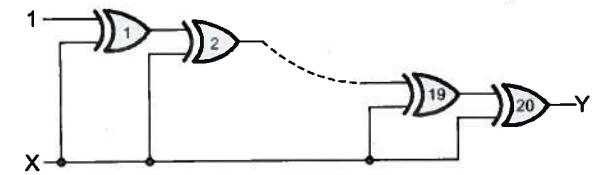
**T2.** Determine the function  $f_3$  if  $f_1 = w\bar{x}z + y\bar{z} + x\bar{z}$  and the overall transmission function of the given logic circuit is to be  $f(w, x, y, z) = \Sigma m(1, 3, 5, 6, 9, 12, 13)$



- (a)  $f_3 = \Sigma m(0, 2, 4, 7, 8, 10, 11, 14, 15)$   
 (b)  $f_3 = \Sigma m(6, 9, 12)$   
 (c)  $f_3 = \Sigma m(0, 2, 4, 7, 8, 10, 11, 14, 15) + d(6, 9, 12)$   
 (d)  $f_3 = \Sigma m(6, 9, 12) + d(0, 2, 4, 7, 8, 10, 11, 14, 15)$

[Ans: (c)]

**T3.** In input to digital circuit consisting of a cascade of 20 EXOR gates is 'X' then output 'Y' is:



- (a) 0 (b) 1  
 (c)  $\bar{X}$  (d)  $X$

[Ans: (b)]

**T4.** Define the connective \* for the Boolean variables X and Y as  $X * Y = XY + X'Y'$ . Let  $Z = X * Y$ . Consider the following expressions P, Q and R.

$$P : X = Y * Z$$

$$Q : Y = X * Z$$

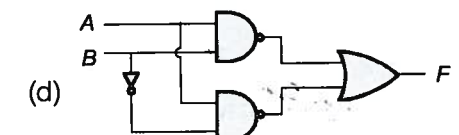
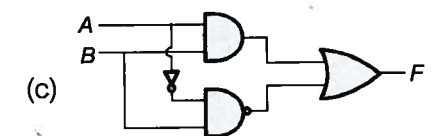
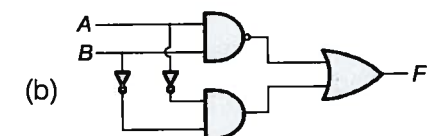
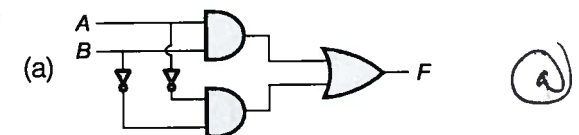
$$R : X * Y * Z = 1$$

Which of the following is TRUE?

- (a) Only P and Q are valid  
 (b) Only Q and R are valid  
 (c) Only P and R are valid  
 (d) All P, Q, R are valid.

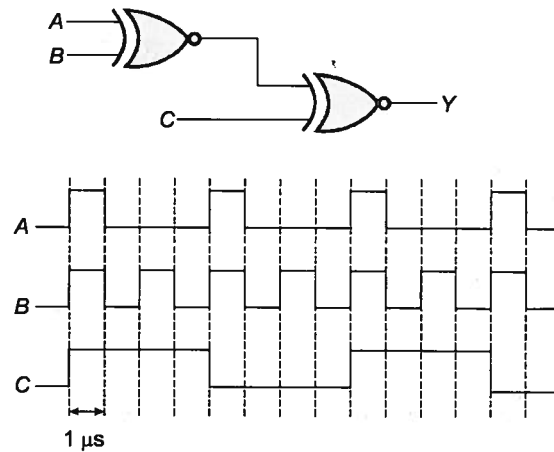
[GATE-2007, Ans: (d)]

**T5.** Which one of the following figures represents the coincidence logic?



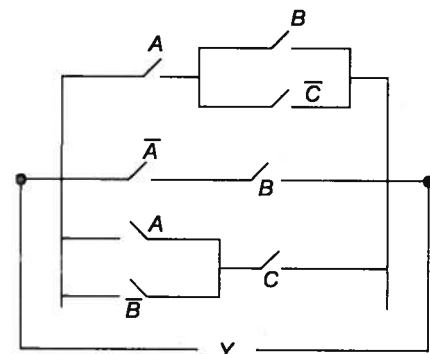
[ESE-2000]

- T6. If the waveforms A, B, C shown in figure below are applied to the Ex-NOR gates. Find the frequency of output.



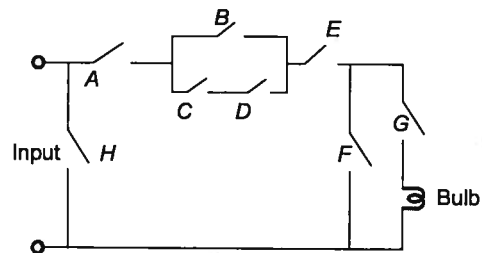
[Ans: 125 kHz]

- T7. Minimized expression for Y is



- (a)  $A + B + C$  (b)  $A + BC$   
(c)  $A + \bar{B}C$  (d)  $\bar{A} + \bar{B} + \bar{C}$

- T8. A switching circuit is given below. Based on this circuit find the Boolean expression for the bulb.



- T9. A Boolean function  $f$  of two variables  $x$  and  $y$  is defined as follows:  
 $f(0, 0) = f(0, 1) = f(1, 1) = 1$ ;  $f(1, 0) = 0$

Assuming complements of  $x$  and  $y$  are not available, a minimum cost solution for realizing  $f$  using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

- (a) 1 unit (b) 4 unit  
(c) 3 unit (d) 2 unit [GATE-2004]

- T10. A  $T$  gate is having the output  $T(A, B) = \bar{A}B$ . Which of the following is/are have about  $T$  gate.

- (a)  $\{T\}$  is functionally complete  
(b)  $\{T, 1\}$  is functionally complete  
(c)  $\{T, 0\}$  is functionally complete  
(d) both a and b

[Ans: (b)]

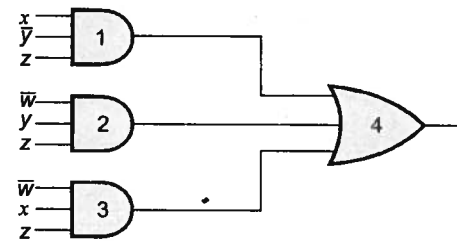
- T11. The simplification of Boolean expressions.

$$a + \bar{a}b + \bar{a}\bar{b}c + \dots \text{ is}$$

- (a)  $a + \bar{b} + \bar{c} + \dots$  (b)  $\bar{a} + b + \bar{c} + \dots$   
(c)  $a + b + \bar{c} + \dots$  (d)  $a + b + c + \dots$

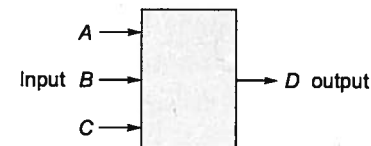
[Ans: (d)]

- T12. The following labelled 1, 2, 3 and 4 in the network shown in the figure is redundant \_\_\_\_\_.



[ESE-1999]

- T13. For the box shown the output  $D$  is true if and only if a majority of the inputs are true.



The Boolean function for the output is

- (a)  $D = AB\bar{C} + \bar{A}BC + A\bar{B}C$   
(b)  $D = ABC + \bar{A}BC + A\bar{B}C + AB\bar{C}$   
(c)  $D = \bar{A}\bar{B}\bar{C} + AB + AC + BC$   
(d)  $D = \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC$

[ESE-2013]

- T14. What is the Boolean expression for the truth table shown below?

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
f	0	0	0	1	0	0	1	0

- (a)  $B(A + C)(\bar{A} + \bar{C})$   
(b)  $B(A + \bar{C})(\bar{A} + C)$   
(c)  $\bar{B}(A + C)(\bar{A} + C)$   
(d)  $\bar{B}(A + C)(\bar{A} + \bar{C})$

[GATE-2006]

- T15. A bank has 3 locks with 1 key for each lock. Each key is owned by a different person. In order to open the vault atleast two people must insert their keys into the assigned locks. All the keys are not inserted at the same time. If the system is to be designed with only two input NAND gates, then find the number of NAND gates required.

[Ans: 6]

- T16. A logic circuit implements the following Boolean function:

$$F(A, B, C, D) = \bar{A}C + A\bar{C}D$$

It is found that  $m$  the circuit the input combination  $A = C$  can never occur. Find a simpler expression for  $F$ .

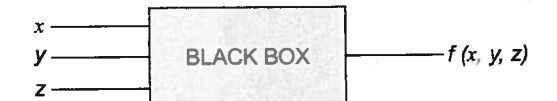
[ESE-2014]

- T17. The standard sum of products of the function  $f = A + B'C$  is expressed as:

- (a)  $\Sigma m(1, 4, 5, 6, 7) + d(2, 3)$   
(b)  $\Sigma m(1, 4, 5, 6, 7)$   
(c)  $\Sigma m(0, 2, 3) + d(1, 4, 5, 6, 7)$   
(d)  $\Pi M(1, 4, 5, 6, 7)$

[DRDO-2008]

- T18. The black box in the above figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates. The function  $f(x, y, z) = 1$  whenever  $x, y$  are different and 0 otherwise. In addition the 3 inputs  $x, y, z$  are never all the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit?



- (a)  $x'y + xy'$  (b)  $x + y'z$   
(c)  $x'y'z' + xy'z$  (d)  $xy + y'z + z'$

[GATE-2007]

- T19. A logic circuit has 3 inputs A, B, C and one output Y. The output is logic 1 when majority number of inputs are at logic 1. Find minimized expression for output Y.

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