DACs and ADCs

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Digital to Analog Converter (DAC)

Specification of DAC

1. Resolution

Resolution of DAC is change in analog voltage corresponding to LSB bit increment at the input.

$$\text{Resolution} = \frac{V_r}{2^n - 1}$$

where, V_r = Reference voltage corresponding to logic 1

n = Number of bit

2. Analog Output Voltage

- Resolution × Decimal equivalent of binary data.
- Analog output voltage of an N-bit straight binary DAC

$$V_0 = K\left[2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \ldots\ldots\ldots + 2^2 b_2 + 2^1 b_1 + b_0\right]$$

where, K = Proportionality factor.

b_n = 1; if the n^{th} bit of digital input is '1'.

= 0; if the n^{th} bit of digital input is '0'.

- Full scale output (V_{FS}) voltage is maximum output of DAC

$$V_{FS} = \text{Resolution} * \text{Maximum decimal}$$

$$= \frac{V_r}{2^n - 1} * (2^n - 1)$$

$$V_{FS} = V_r$$

3. % Resolution

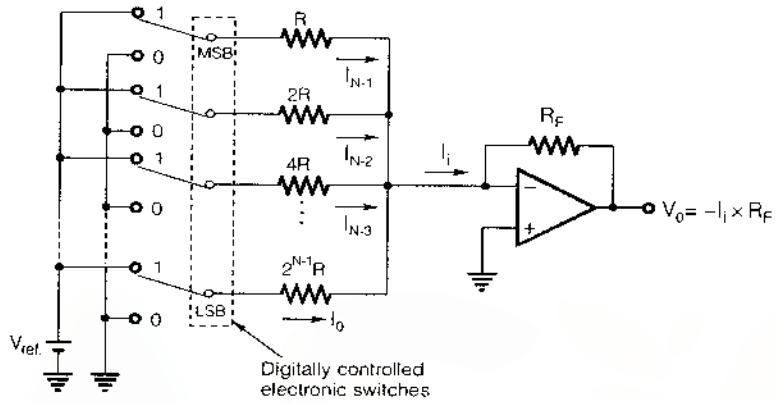
$$\% \text{ Resolution} = \frac{\text{Resolution}}{V_{FS}} \times 100$$

$$\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100$$

4. Error/Accuracy

Maximum error acceptable in ADC/DAC is 1 LSB bit which is equal to resolution.

Weighted-Resistor DAC



Output voltage:

$$V_0 = \frac{R_F}{2^{N-1} \cdot R}\left(2^{N-1} V_{N-1} + 2^{N-2} V_{N-2} + \ldots\ldots + 2^1 V_1 + 2^0 V_0\right)$$

Proportionality factor:

$$K = \frac{R_F}{2^{N-1} \cdot R} \cdot V_R$$

Input current to OP-AMP:

$$I_i = \frac{V_{ref.}}{2^{N-1} \cdot R} \sum_{i=0}^{N-1} 2^i b_i$$

Maximum output current:

$$I_{max} = \frac{V_{ref.}}{2^{N-1} \cdot R}\left(2^N - 1\right)$$

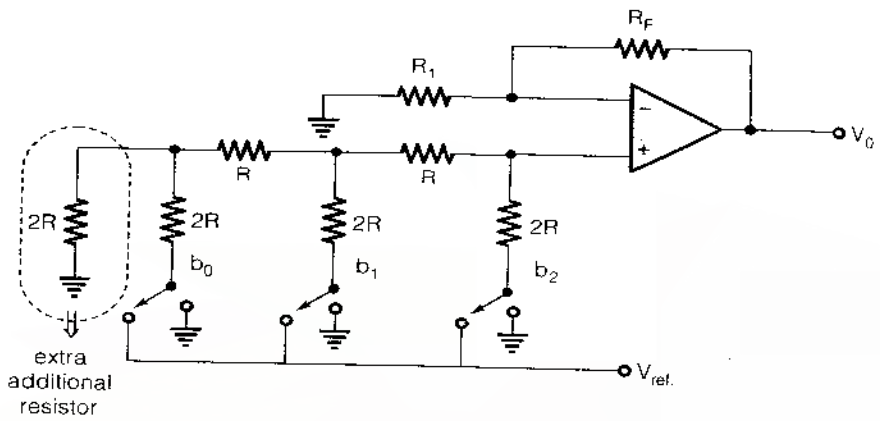
Resistance:

$$\text{LSB Resistance} = (2^{N-1}) \times \text{MSB Resistance}$$

Remember:

- The resistance values are weighted in accordance with the binary weight.
- Here "OP-AMP" is employed as a "summing amplifier".
- OP-AMP is used in negative feedback mode to work as a "current to voltage converter".
- For N-bit DAC
  - (i) Number of different levels = 2^N
  - (ii) Number of steps = $2^N - 1$

R-2R Ladder DAC by Using Non-inverting OP-AMP



3-bit (b_2 b_1 b_0) R-2R ladder DAC

Gain of OP-AMP :

$$\frac{V_0}{V_{ref.}} = \left(1 + \frac{R_F}{R_1}\right)$$

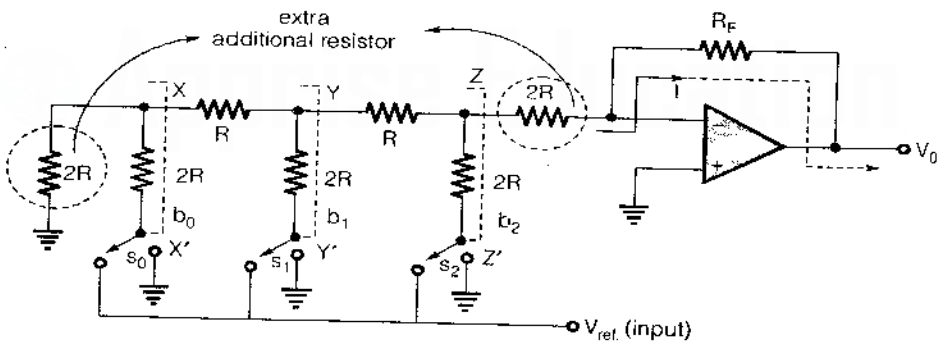
where $V_{ref.}$ = Reference voltage or Input voltage

V_0 = Output voltage

Output analog voltage:

$$V_0 = \frac{V_{ref.}}{2^N}\left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \left[1 + \frac{R_F}{R_1}\right]$$

R-2R Ladder DAC by Using Inverting OP-AMP



3-bit (b_2 b_1 b_0) R-2R ladder DAC

Output voltage:

For 3-bit DAC

$$V_0 = -\left(\frac{R_F}{3R}\right)\left(\frac{V_{ref.}}{2^3}\right)[4b_2 + 2b_1 + b_0]$$

For N-bit DAC

$$V_0 = \frac{V_{ref.}}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \left[\frac{-R_F}{3R}\right]$$

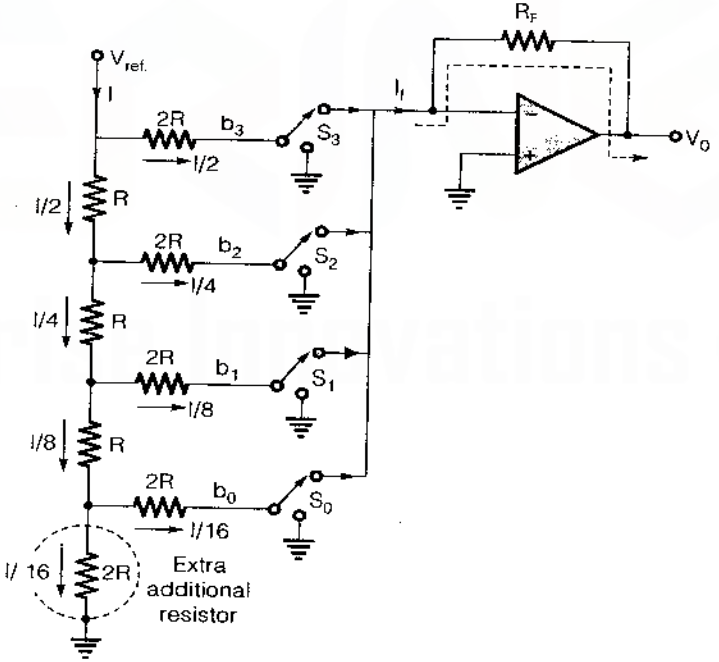
Output current:

$$I = \frac{V_{ref.}}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \left[\frac{1}{3R}\right]$$

Remember:

Resolution of R-2R ladder network is $\frac{V_r}{2^n}$.

Inverted Ladder (R-2R)type DAC



Output voltage:

For 4-bit DAC

$$V_0 = \frac{V_{ref.}}{2^4}[b_0 + 2b_1 + 4b_2 + 8b_3]$$

For N-bit DAC

$$V_0 = \frac{V_{ref.}}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \left(\frac{-R_F}{R}\right)$$

Forward current :

$$I_f = \frac{V_{ref.}}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \frac{1}{R}$$

Note:

- ON-OFF Switches (S_0, S_1, S_2, S_3) are at the same potential.
- We always consider the bit as MSB, where the input reference voltage or supply to be given.
- The bit stream $(b_3\, b_2\, b_1\, b_0)_2$ has MSB = b_3 and LSB = b_0.

Analog to Digital Converter

Specifications of ADC

1. Voltage Range

$$\text{Voltage range} = V_{max} - V_{min}$$

2. Resolution

$$\text{Resolution} = \frac{V_{range}}{2^n - 1}$$

$$\%\ \text{Resolution} = \frac{1}{2^n - 1} \times 100$$

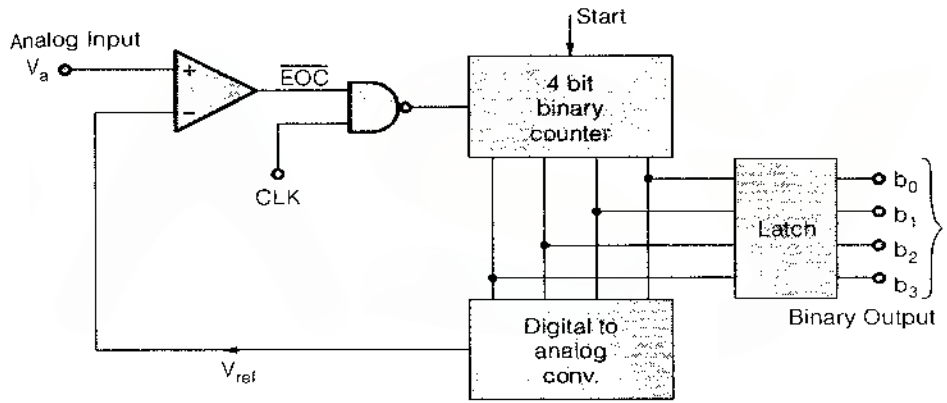
3. Dynamic range

$$\text{Dynamic range} = (1.8 + 6n)\ \text{dB}$$

Types of ADCs are

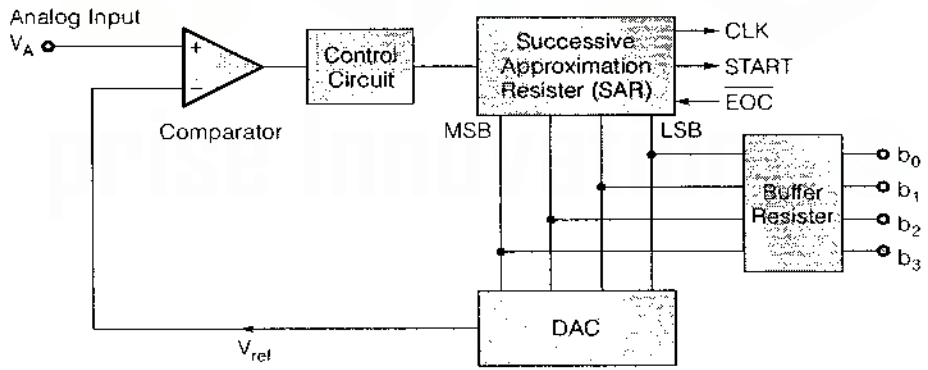
(a) Counter type
(b) Successive approximation resistor type (SAR)
(c) Flash type
(d) Dual slope type

(a) Counter type ADC



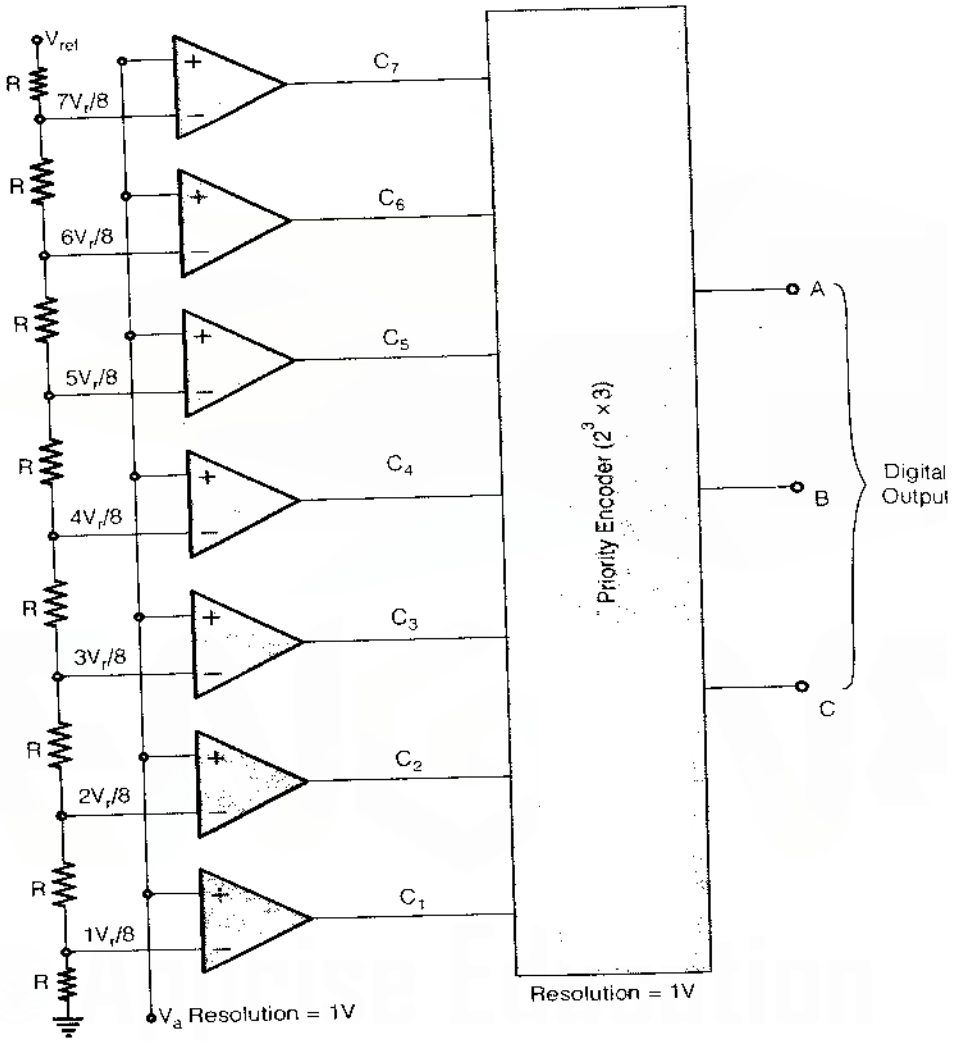
- Number of clock pulse required for n-bit conversion = $2^n - 1$
- Maximum conversion time = $(2^N - 1)\, T_{clk}$.
- Counter type ADC also known as 'ramp type' ADC.
- In this ADC, conversion time depends on input analog voltage.

(b) SAR type ADC



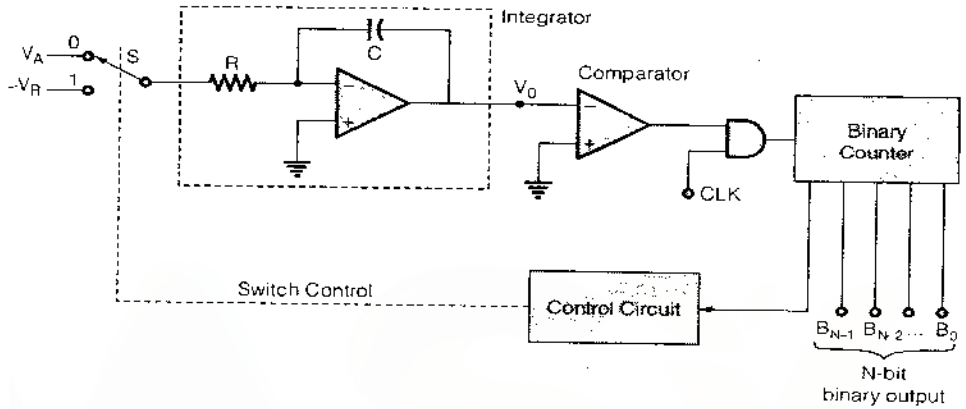
- Number of clock pulse required for n-bit conversion = n.
- Maximum conversion time = $n * T_{clk}$.
- In SAR ADC, conversion time is independent of input analog voltage.

(c) Flash type ADC



- For n bit conversion flash type ADC requires
  - (i) $2^n - 1$ comparators
  - (ii) 2^n resistors
  - (iii) One $2^n \times n$ priority encoder
- It is the fastest ADC among all.
- It is also known as parallel comparator type ADC.

(d) Dual slope integrating type ADC



- Total number of clock pulse required = $2^n + N \approx 2^{n+1}$.
- It is most accurate ADC therefore mostly used in digital voltmeter.
- It is slowest ADC.

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