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Electronic Devices

We know that, the solids can be classified in three types as per their electrical conductivity (i) Conductors, (ii) Insulators and (iii) Semiconductors.

Conductors are those in which electric charges can flow easily, while semiconductor are those whose conductivity is intermediate between conductors and insulators. These can be divided on the basis of conductivity and energy band.

IN THIS CHAPTER ....

- Energy Bands in Solids
- Types of Semiconductors
- Semiconductor Diode or *p-n* Junction Diode
- Diode as a Rectifier
- Special Types of *p-n* Junction Diode
- Junction Transistor
- Biasing of Transistor
- Transistor Circuit Configurations
- Transistor as an Amplifier
- Transistor as an Oscillator
- Logic Gates
- Combination of Logic Gates

Energy Bands in Solids

Inside the crystal of a solid, each electron has a unique position and no two electrons see exactly the same pattern of surrounding charges. Because of this, each electron will have a different energy level. These different energy levels with continuous energy variation are called *energy bands*.

These bands are of two types

(i) **Valence band** is the range of energies possessed by the valence electrons.

(ii) **Conduction band** is the range of energies possessed by the conduction electrons.

Note With no external energy, all the valence electrons will reside in the valence band.

Energy Band Gap

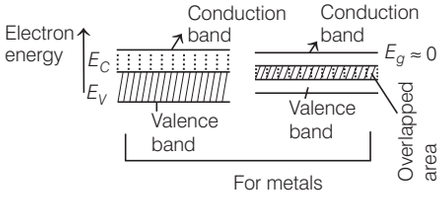
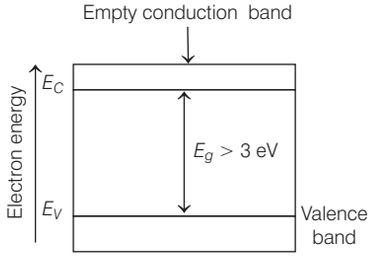
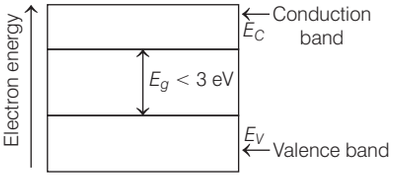
It is the gap between the top of the valence band and the bottom of the conduction band.

i.e. $E_g = E_c - E_v$

It may be zero, small or large depending upon the material. Also, no free electrons are present in this gap.

As the temperature increases, energy band gap decreases.

Difference between Conductor, Insulator and Semiconductor on the basis of Conductivity and Energy Bands

Conductor (Metal)	Insulator	Semiconductor
Conductivity (σ) lies in the range of 10^4 -$10^7 \Omega^{-1}m^{-1}$.	Conductivity (σ) lies in the range of 10^{-20} -$10^{-10}\Omega^{-1}m^{-1}$.	Conductivity (σ) lies in the range of 10^{-6} -$10^4\Omega^{-1}m^{-1}$.
In conductor, either there is no energy gap between the conduction band which is partially filled with electrons and valence band or the conduction band and valence band overlap each other. 	In insulator, the valence band is completely filled, the conduction band is completely empty. In this, energy gap is quite large and even energy from any other source cannot help electrons to overcome it. 	In semiconductor, the valence band is totally filled and the conduction band is empty but the energy gap between conduction band and valence band is very small. Thus, at room temperature, some electrons in the valence band acquire thermal energy greater than energy band gap and jump over to the conduction band where they are free to move under the influence of even a small electric field and acquire small conductivity. 
Current carrier Free electrons	—	**Current carriers** Free electrons and holes (a vacancy created when an e^- leaves an carries positive charge)

Types of Semiconductors

On the basis of purity, semiconductors are classified into two types

1. Intrinsic Semiconductors

These are pure semiconductor without any impurity, *e.g.* silicon, germanium, etc. At room temperature, intrinsic semiconductor has equal number of holes and electrons.

i.e. $n_e = n_h = n_i$

where, n_i is called *intrinsic carriers concentration.*

The conductivity of intrinsic semiconductors is due to both holes and electrons. The free electrons moves completely independently as conduction electron and give rise to an electron current I_e, under applied field. Similarly, under the effect of field, holes moves towards negative potential giving rise to hole current I_h.

So, total current, $I = I_e + I_h$

At equilibrium, $n_e n_h = n_i^2$

This is known as **mass-action law**.

At $T = 0$ K, it behaves as an insulator. However, at $T > 0$ K, some electrons excite to the conduction band, leaving equal number of holes there.

2. Extrinsic Semiconductors

When a small quantity of impurity is added in a pure or intrinsic semiconductor (nearly 1 atom of impurity in 10^7 atoms of pure semiconductor), the conductivity of semiconductor increases. Such an impure semiconductor is called *extrinsic* or *doped semiconductor*.

Depending upon the nature of impurity added in intrinsic semiconductor, the extrinsic semiconductors are of two types

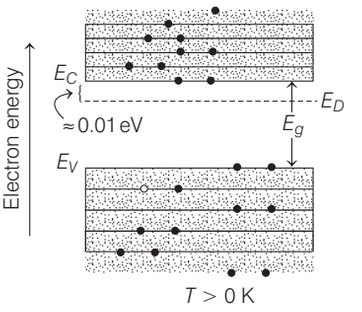
(i) *n*-type and (ii) *p*-type

n-type Semiconductors

When a small quantity of pentavalent impurity such as antimony (Sb) or arsenic (As), etc., is introduced in pure germanium (or silicon) crystal, then *n*-type semiconductor is formed. The pentavalent impurity is also called **donor atoms** as they donate conduction electrons to crystal.

Following are important points regarding *n*-type semiconductors

- Electrons are majority charge carriers and holes are minority charge carriers or number of electrons are much greater than the number of holes, *i.e.* $n_e >> n_h$; $I_e >> I_h$
- These type of semiconductors are electrically neutral.
- Conductivity, $\sigma \simeq n_e \mu_e e$
- Energy band gap of *n*-type semiconductor at $T > 0$ K is



p-type Semiconductors

When a small quantity of a trivalent impurity such as indium (In), boron (B) aluminium (Al), etc., having three valence electrons is introduced into the pure germanium, then such type of semiconductors are called *p-type* or *acceptor type semiconductors*.

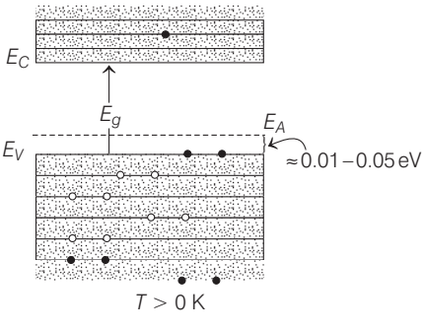
This hole is equivalent to a positively charged particle. Since, positive holes are responsible to increase the conductivity in this crystal, the crystal so obtained is called the *p-type crystal* and the impurity atom is called *acceptor impurity*.

Following are important points regarding *p*-type semiconductors

- Holes are majority charge carriers and electrons are minority charge carriers or number of holes are much greater than the number of electrons.

$$n_h >> n_e;\ I_h > I_e$$

- These types of semiconductors are electrically neutral.
- Conductivity, $\sigma \simeq n_h \mu_h e$
- Energy band gap of *p*-type semiconductors at $T > 0$ K is



Note Generally, when a battery is connected across a semiconductor (whether intrinsic or extrinsic), conductivity is given as $\sigma = n_e e\mu_e + n_h e\mu_h$.

Example 1. *A pure Si crystal has 5×10^{28} atoms m^{-3}. It is doped by 1 ppm concentration of pentavalent As. The number of holes is (approx) (Given, $n_i = 1.5 \times 10^{16}\ m^{-3}$)*

(a) $2.2 \times 10^6\ m^{-3}$ ***[NCERT]***
(b) $4.5 \times 10^9\ m^{-3}$
(c) $6.2 \times 10^6\ m^{-3}$
(d) $8.1 \times 10^9\ m^{-3}$

Sol. (*b*) 1 ppm concentration of As means 1 atom of Si is doped out of 10^6 atoms.

$\Rightarrow$ Number of doped atoms in 5×10^{28} atoms

$$= \frac{5 \times 10^{28}}{10^6} = 5 \times 10^{22} \text{ atoms}$$

Since, 1 As atom donates one electron, hence number of excess electrons $= 5 \times 10^{22} = n_e$

i.e. $n_e = 5 \times 10^{22}$

According to law of mass action,

$$n_e \cdot n_h = n_i^2$$

$$\Rightarrow \quad n_h = \frac{n_i^2}{n_e} = \frac{(1.5 \times 10^{16})^2}{5 \times 10^{22}}$$

$$= 4.5 \times 10^9\ m^{-3}$$

$\therefore$ Number of holes formed $= 4.5 \times 10^9\ m^{-3}$

Example 2. *Determine the number of donor atoms which have to be added to an intrinsic germanium semiconductor to produce an n-type semiconductor of conductivity $5\,\Omega^{-1}\,cm^{-1}$.*

Given that, the mobility of electrons in n-type Ge is $3900\ cm^2V^{-1}s^{-1}$. Neglect the contribution of holes to conductivity. (Take, charge on electron, $e = 1.6 \times 10^{-19}$ C)

(a) $8.013 \times 10^{21}\ m^{-3}$ (b) $6.2 \times 10^{20}\ m^{-3}$
(c) $5.3 \times 10^{19}\ m^{-3}$ (d) $4.8 \times 10^{18}\ m^{-3}$

Sol. (*a*) Here, $e = 1.6 \times 10^{-19}$ C,

$$\sigma = 5\ \Omega^{-1}\ cm^{-1} = 500\ \Omega^{-1}\ m^{-1},$$

$$\mu_e = 3900\ cm^2\ V^{-1}s^{-1} = 0.39\ m^2V^{-1}s^{-1}$$

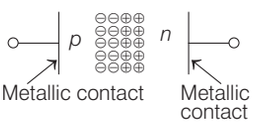
Now, $\sigma = en_e\mu_e$ (neglecting contribution of holes)

$\therefore$ $$n_e = \frac{\sigma}{e\mu_e} = \frac{500}{1.6 \times 10^{-19} \times 0.39}$$

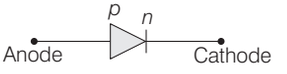
$$= 8.013 \times 10^{21}\ m^{-3}$$

Semiconductor Diode or *p-n* Junction Diode

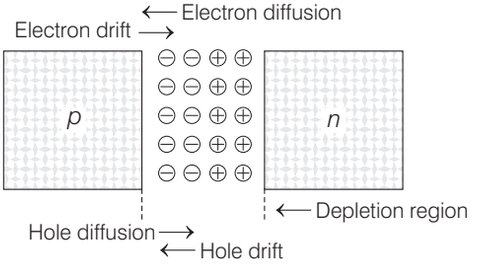
When a *p*-type semiconductor is brought into a close contact with *n*-type semiconductor crystal, the resulting arrangement is called a semiconductor diode or *p-n* junction diode.



(a) Semiconductor diode



(b) Symbol for *p-n* junction diode

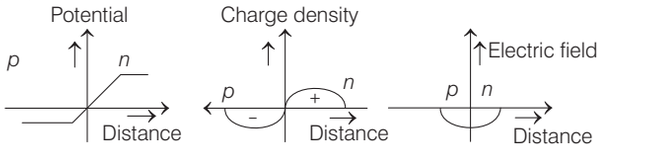


p-n junction formation process

On account of difference in concentration of charge carriers in the two sections of *p-n* junction, the electrons from *n*-region diffuse through the junction into *p*-region and the holes from *p*-region diffuse into *n*-region.

Due to this diffusion, the neutrality of the concentration of charge carriers on p and n-type semiconductors is disturbed. Due to which a layer of negative charge ions appear near the junction of p-type crystal and a layer of positive ions appears near the junction of n-type crystal. This layer is called **depletion region**. Also, this causes a difference of potential across the junction of two regions. This potential tends to prevent the movement of electrons from n-region to p-region and is often called **barrier potential**.

Few important graphs related to potential barriers are as follows



(a) Potential *versus* distance (b) Charge density *versus* distance (c) Electric field *versus* distance across the depletion region

Diffusion and Drift Currents

Current across the p-n junction are of two types

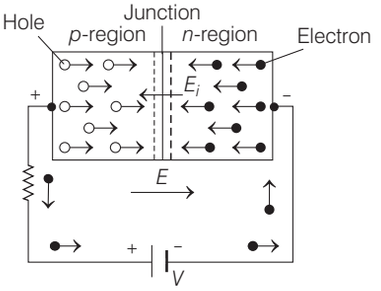
(i) **Diffusion Current (I_{df})** It is the current flowing from p-side to n-side due to the diffusion of electrons and holes because of concentration difference.

(ii) **Drift Current (I_{dr})** It is the current flowing due to electron-hole pairs under the influence of an external electic field.

Biasing of Junction Diode

Biasing is the method of connecting external battery or emf source to a p-n junction diode. The diode can be connected to an external battery in following two ways

(i) **Forward Biasing** A p-n junction is said to be forward biased, if the positive terminal of the external battery B is connected to p-side and the negative terminal to the n-side of p-n junction.

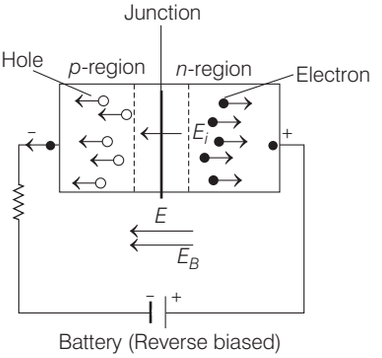


Forward biased p-n junction diode

Following are few important points related to forward biasing

- An electric current flow due to migration of majority carriers across the p-n junction; which is called **forward current**. Since, the small increase in forward voltage shows the large increase in forward current hence, the resistance of p-n junction is low to the flow of current when forward biased.
- The effective barrier height under forward bias is $V_0 - V$.
- Width of the depletion layer decreases.
- Total diode forward current is the sum of hole diffusion current and convential current of electron diffusion. The magnitude of current is in mA.
- The voltage at which current starts to increase is called **cut in (knee) voltage**. For Ge, it is 0.3 V and for Si, it is 0.7 V.

(ii) **Reverse Biasing** A p-n junction is said to be reverse biased, if the positive terminal of the external battery B is connected to n-side and the negative terminal to p-side of the p-n junction.



Battery (Reverse biased)

Following are few important points related to reverse biasing.

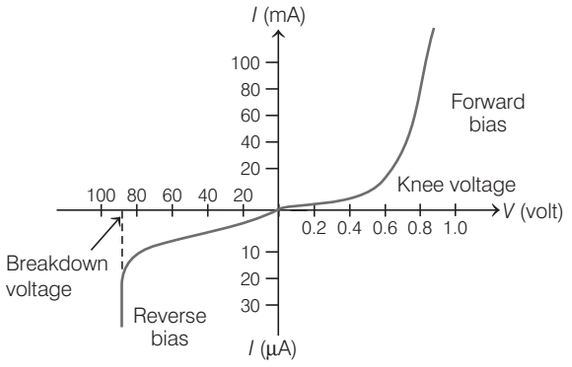
- A few minority carriers (holes in n-section and electrons in p-section) of p-n junction diode cross the junction after being accelerated by high reverse bias voltage. They constitute a current that flows in the opposite direction, this is called **reverse current of leakage current**. Since, the large increase in reverse voltage shows small increase in reverse current, hence the resistance of p-n junction is high to the flow of current when reverse biased.
- The direction of applied voltage is same as the direction of barrier potential. So, effective barrier height will be $(V_0 + V)$.
- Width of the depletion layer increases.
- The current under reverse bias is essentially voltage independent upto a critical reverse bias voltage, known as *breakdown voltage* (V_{br}).

  When $V = V_{br}$, the reverse current increases sharply.

I-V Characteristics of a Diode

The voltage-current characteristics curves of a p-n junction diode are graphs showing the change in current flowing through the junction with change in an applied

voltage when junction is forward and reverse biased. It is as shown below.



Diode Resistance

(i) **Static or DC Resistance of Diode** In forward biasing, the ratio of potential applied to the junction diode to the current corresponding to it, is called static or DC resistance of diode.

Thus, $r_{DC} = \frac{V}{I}$

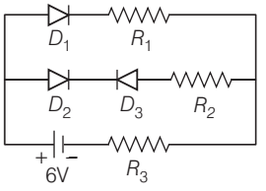
Its unit is ohm (Ω).

(ii) **Dynamic or AC Resistance of Diode** In forward bias, the reciprocal of the slope of characteristic curve or ratio of small change in voltage ΔV to a small change in current ΔI is called dynamic or AC resistance of diode.

Thus, $r_{AC} = \frac{\Delta V}{\Delta I}$

Its unit is ohm (Ω) .

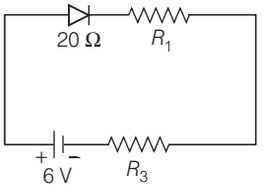
Example 3. *Figure shows a circuit in which three identical diodes are used. Each diode has forward resistance of* 20 Ω *and infinite backward resistance. Resistors,* $R_1 = R_2 = R_3 = 50\ \Omega$ *and battery voltage is* 6 V. *The current through* R_3 *is*



(a) 50 *mA* *(b)* 100 *mA* *(c)* 60 *mA* *(d)* 25 *mA*

Sol. (*a*) As diode is conducting in forward bias condition and not conducting in reverse bias condition. Diode D_1 is in forward bias, and diode D_2 is in forward bias but D_3 is reverse bias. So the figure can be drawn as

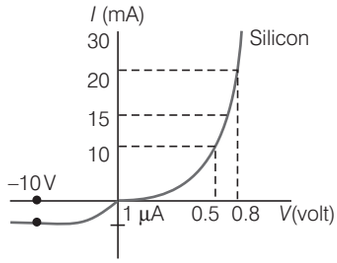
Here, 20 Ω, $R_1\Omega$ and $R_3\Omega$ are in series.



Equivalent resistance = 50 + 50 + 20 = 120 Ω

$\therefore \quad I = \frac{V}{R} = \frac{6}{120} = \frac{1}{20} \Rightarrow I = 50$ mA

Example 4. *The V-I characteristic of silicon diode is shown in the figure. The resistance of the diode at* $V_D = -10\ V$ *is*



(*a*) 10 Ω (*b*) 20 Ω
(*c*) 10^{12} Ω (*d*) 10^7 Ω

Sol. (*d*) From the curve, at $V = V_D = -10$ V, $I = -1\mu$A

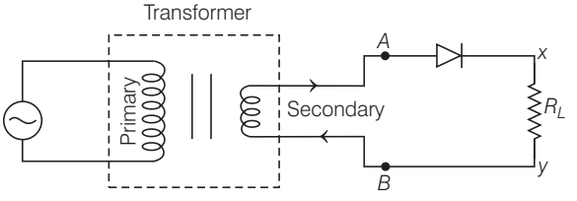
$\therefore \quad R = \frac{10\ \text{V}}{1\mu\text{A}} = 1 \times 10^7\ \Omega = 10^7\ \Omega$

Diode as a Rectifier

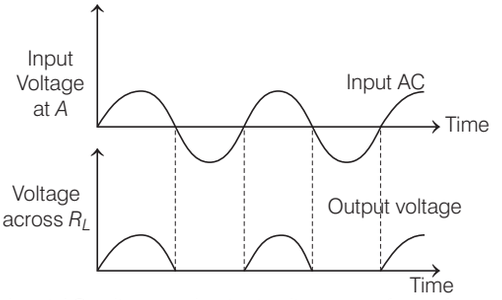
Junction diode allows current to pass only when it is forward biased. So, if an alternating voltage is applied across a diode, the current flows only in that part of the cycle, when the diode is forward biased. This property is used to rectify alternating voltages and the circuit used for this purpose is called a **rectifier** and the process is known as **rectification**.

Half-Wave Rectifier

It is a circuit in which voltage is applied across a diode in series with a load. A pulsating voltage will appear across the load during the half cycle of the AC input when diode is forward biased.



Half-wave rectifier circuit



Input AC voltage and output voltage waveforms from the half-wave rectifier circuit

Important Points Related to Half-Wave Rectifier

- **Average output** in one cycle

$$I_{DC} = \frac{I_0}{\pi} \text{ and } V_{DC} = \frac{V_0}{\pi};\ I_0 = \frac{V_0}{r_f + R_L},$$

$$V_{DC} = \frac{V_0}{\pi\left(1 + \frac{r_f}{R_L}\right)} \quad (r_f = \text{forward biased resistance})$$

- **rms output** $I_{rms} = \frac{I_0}{2}, V_{rms} = \frac{V_0}{2}$
- The ratio of the effective alternating component of the output voltage or current to the DC component is known as **ripple factor**.

$$r = \frac{I_{AC}}{I_{DC}} = \left[\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1\right]^{1/2} = 1.21$$

The smaller the ripple factor, more effective will be the rectifier.

- **Peak inverse voltage** (PIV) The maximum reverse biased voltage that can be applied before commencement of Zener region is called the peak inverse voltage. When diode is not conducting, PIV across it = V_0.
- **Efficiency** It is given by

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{40.6\%}{1 + r_f/R_L}$$

If $R_L >> r_f$, then $\eta = 40.6\%$ and if $R_L = r_f$, then $\eta = 20.3\%$.

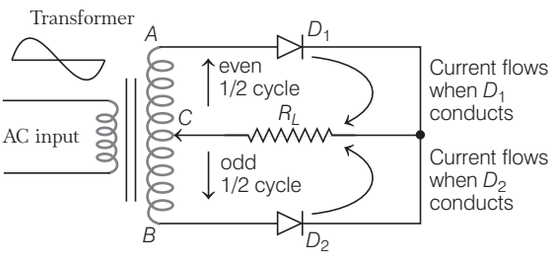
- The ratio of i_{rms} and i_{DC} is known as **form factor**.

$$\text{Form factor} = \frac{I_{rms}}{I_{DC}} = \frac{\pi}{2} = 1.57$$

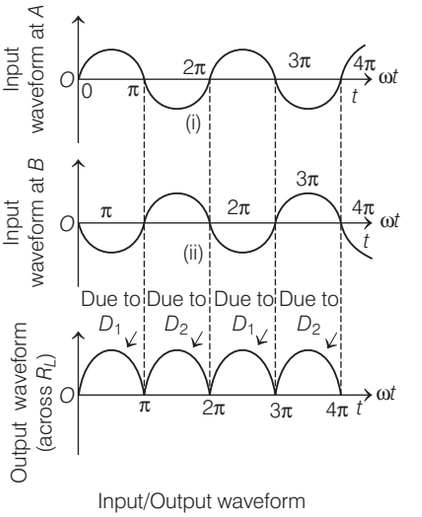
- The ripple frequency (ω) for half-wave rectifier is same as that of AC.

Full Wave Rectifier

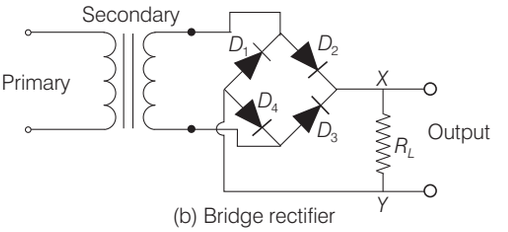
It is a circuit which gives output rectified voltage corresponding to both the positive as well as negative half of the AC cycle. These can be of two types namely: centre-tap full wave rectifier and full wave bridge rectifier.



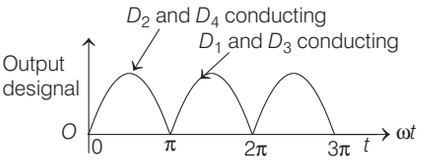
(a) Centre-tap full wave rectifier



Input/Output waveform



(b) Bridge rectifier



(c) Output waveforms for a bridge rectifier

Important Points Related to Full Wave Rectifier

- Output voltage is obtained across the load resistance R_L. It is not constant but pulsating in nature.
- **Average output**

$$V_{av} = \frac{2V_0}{\pi}, I_{av} = \frac{2I_0}{\pi}, V_{DC} = \frac{2V_0}{\pi\left(1 + \frac{r_f}{R_L}\right)}$$

- **rms output** $V_{rms} = \frac{V_0}{\sqrt{2}}, I_{rms} = \frac{I_0}{\sqrt{2}}$
- **Ripple factor** $r = 0.48 = 48\%$
- **Ripple frequency** The ripple frequency of full wave rectifier

$= 2 \times$ Frequency of input AC

- **Peak inverse voltage (PIV)** Its value is $2V_0$.
- **Efficiency** $\eta_{\%} = \frac{81.2}{1 + \frac{r_f}{R_L}}$ for $r_f << R_L, \eta = 81.2\%$
- **Form factor**, $f = \frac{I_{rms}}{I_{DC}} = \frac{\pi}{2\sqrt{2}}$

Special Types of *p-n* Junction Diode

Junction diodes are of many types and they have a wide range of applications, few of them are discussed as below.

Optoelectronic Junction Devices

Semiconductor diodes in which carriers are generated by photons (photoexcitation) are called optoelectronic devices, *e.g.* photodiodes, LED, solar cell, etc.

Light Emitting Diodes (LED)

It is a heavily doped forward biased *p-n* junction diode which emits light when recombination of electrons and holes takes place at the junction.

The colour of the light emitted depends upon the types of material used in making the semiconductor diode.

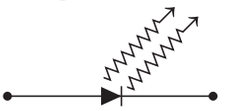
(i) Gallium-Arsenide (Ga-As) — Infrared radiation

(ii) Gallium-Phosphide (Ga-P) — Red or green light

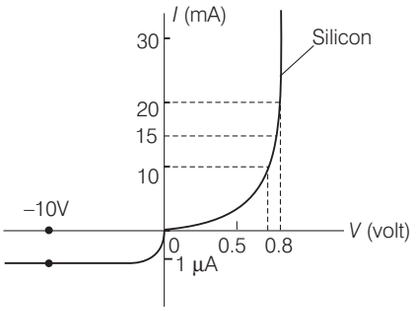
(iii) Gallium-Arsenide-Phosphide (Ga-As-P) — Red or Yellow light

LEDs emit no light when reverse biased, rather it will be destroyed.

Its symbol is shown in figure



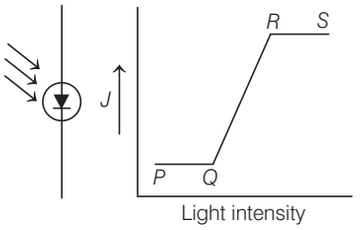
***I-V* Characteristics of LED** Its *I-V* characteristics is similar to that of a Si-junction diode, but the threshold voltages are much higher and slightly different for each colour.



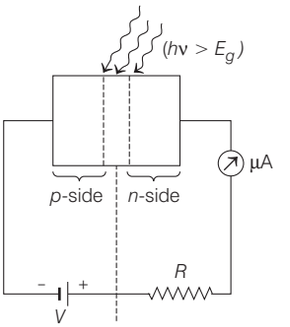
Photodiode

It is a junction diode fabricated with a transparent window to allow light to fall on the diode. It is operated under reverse bias.

Its symbol is given below.

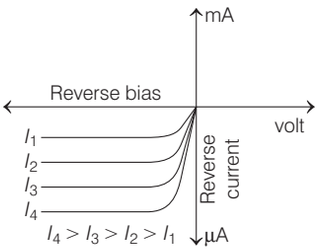


If the photodiode is in forward bias, some current flows in the circuit, shown by the *PQ* portion of the graph, this current *PQ* flows when no light is incident on it, is called **dark current**. When the intensity of light is increased, the current goes on increasing, shown by *QR* portion of the graph. A stage is reached when current does not increase with increase of intensity of light, is called **saturated current**, shown in *RS* portion of the graph.



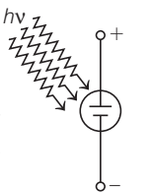
A reverse biased photodiode illuminated with light

***I-V* Characteristics of Photodiode** The characteristics of the photodiode at different intensities are as follows



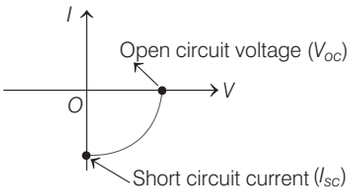
V-I characteristics of photodiode at different intensites

Solar Cell



It is basically a *p-n* junction diode which generates emf when solar radiations falls on it. In this diode, either *p* or *n* section is made very thin (so that the light energy falling on it is not greatly absorbed before reaching the junction). It is used to convert light energy into electric energy. Its symbol is as shown in figure

***I-V* Characteristics of Solar Cell** The *I-V* characteristics of solar cell are shown in the following figure. It is drawn in the fourth quadrant of the coordinate axes, because a solar cell does not draw current but supplies the same to the load.

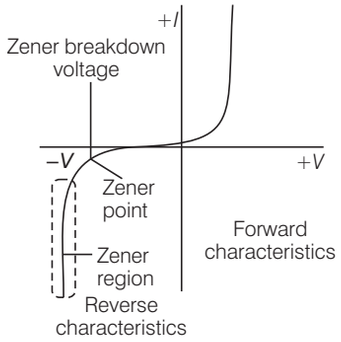


Zener Diode

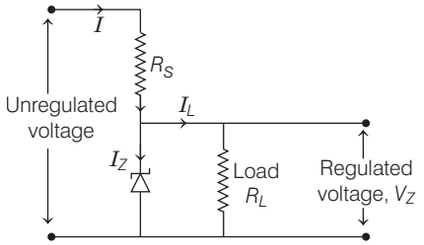
The specially designed junction diodes, which can operate in the reverse breakdown voltage region continuously without being damaged are called *zener diodes*. Symbol for this diode is given below.

***I-V* Characteristics of Zener Diode** The *I-V* characteristics of Zener diode is shown below and we observe that when the applied reverse voltage (V) reaches the breakdown voltage (V_Z) of the Zener diode, there is a large change in the current.

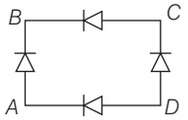
But after the breakdown voltage V_Z, a large change in the current can be produced by almost insignificant change in the reverse bias voltage.



Zener Diode as Voltage Regulator Zener diode can be used as a voltage regulator, in which the constant output voltage is taken across a load resistance connected in parallel with it.

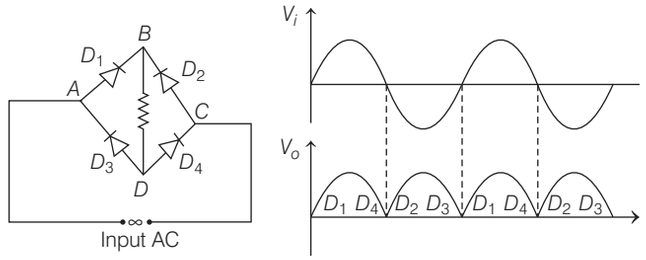


Example 5. *In figure, the input is across the terminals A and C and the output is across B and D. Then the output is*



(a) zero
(b) same as the input
(c) half -wave rectified
(d) *full wave rectified*

Sol. (*d*) AC input is given across the points *A* and C and the output is taken across the points *B* and *D*, which is shown in the following figure.



For positive half cycle, diodes D_1 and D_4 are in forward biased while diodes D_2 and D_3 are in reverse biased.

Similarly, for negative half cycle, diodes D_2 and D_3 are in forward biased and diodes D_1 and D_4 are in reverse biased.

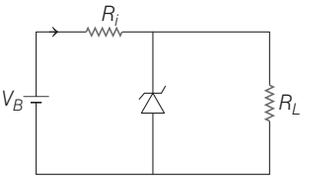
Hence, given circuit is full wave bridge rectifier, which gives full wave rectified output.

Example 6. *A photodiode is a special purpose p-n junction diode fabricated with a transparent window to allow light to fall on the diode. It is operated under* ***[NCERT]***

(a) *forward bias* (*b*) *reverse bias*
(c) *Both reverse and forward bias*
(*d*) *No biasing is required.*

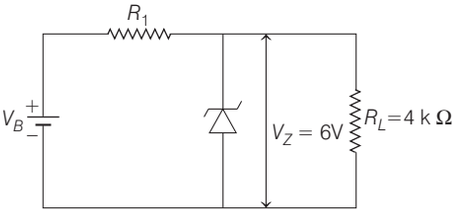
Sol. (*b*) The photodiode is reverse biased for operating in the photoconductive mode. As the photodiode is in reverse bias, the width of the depletion region increases. This reduces the junction capacitance and thereby the response time. In effect, the reverse bias causes faster response time for the photodiode.

Example 7. *The figure represents a voltage regulator circuit using a Zener diode. The breakdown voltage of the Zener diode is 6 V and the load resistance is $R_L = 4\,k\Omega$. The series resistance of the circuit is $R_i = 1k\Omega$. If the battery voltage V_B varies from 8V to 16V, what are the minimum and maximum values of the current through Zener diode?* ***[JEE Main 2019]***



(a) 1.5 *mA*, 8.5 *mA* *(b)* 1 *mA*, 8.5 *mA*
(c) 0.5 *mA*, 8.5 *mA* *(d)* 0.5 *mA*, 6 *mA*

Sol. (c) In given voltage regulator circuit



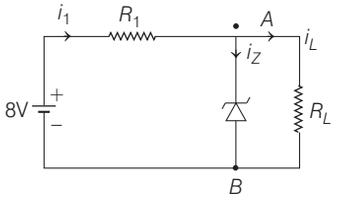
Zener breakdown voltage, $V_Z = 6$ V

So, across R_L, potential drop is always 6 V.

So, current through load resistance is

$$i_L = \frac{V_Z}{R_L} = \frac{6}{4\times10^3} = 1.5\times10^{-3}\ \text{A}$$

Now, when $V_B = 8$ V



Potential drop across $R_1 = 8 - 6 = 2$ V

So, current through R_1 is $i_1 = \frac{V}{R_1} = \frac{2}{1\times10^3} = 2\times10^{-3}$ A

So, current through Zener diode is

$$i_Z = i_1 - i_L = 2\times10^{-3} - 1.5\times10^{-3}$$
$$= 0.5\times10^{-3} \text{ A} = 0.5 \text{ mA}$$

Similarly, when $V_B = 16$ V

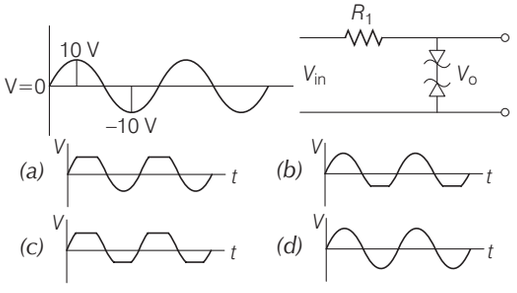
$$V_{R_1} = 16 - 6 = 10 \text{ V}$$

$$\therefore \quad i_1 = \frac{10}{1\times10^3} = 10\times10^{-3} \text{ A}$$

Hence,
$$i_Z = i_1 - i_L = 10\times10^{-3} - 1.5\times10^{-3}$$
$$= 8.5\times10^{-3} \text{ A} = 8.5 \text{ mA}$$

Example 8. *Take the breakdown voltage of the Zener diode used in the given circuit as 6V. For the input voltage shown in figure below, the time variation of the output voltage is (Graphs are drawn schematically and on not to scale)*

[JEE Main 2020]

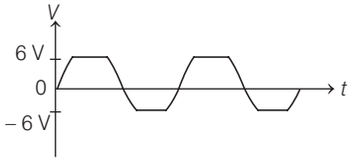


Sol. (c) There are two Zener diodes in reverse polarity. So, if the input voltage changes its polarity, then one Zener diode will be in forward bias and other zener diode will be in reverse bias. This happens at each kind of polarity of input voltage.

Now, if the input voltage is less than 6 V, then output will follow the input voltage, which means it will remain sinusoidal.

And if the input voltage is more than 6 V, the output voltage will remain constant equal to 6 V (as forward biased Zener diode will not be active and reverse biased Zener diode will keep the potential constant across it).

So, we can conclude from available options, that the correct graph is



Hence, correct option is (c).

Junction Transistor

A junction transistor is a three terminal device which is formed by sandwiching a thin wafer of one type of semiconductors between two layers of another type.

It is of two types : *n-p-n* and *p-n-p*

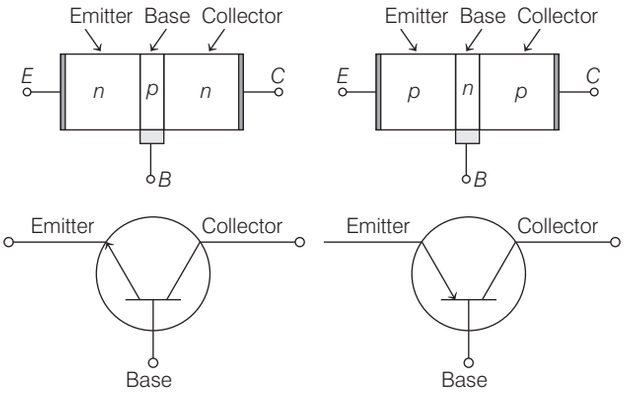
The there terminals of transistor are emitter, base and the collector.

Emitter (*E*) It is heavily doped and of moderate size as it emits the majority charge carriers into the base by which current flows in the transistor.

Base (*B*) The base region is very lightly doped and thin. Most of the charge carriers emitted by the emitter pass through it to the collector.

Collector (*C*) The doping level of collector is neither very high nor very low, however it lies between the doping levels of emitter and base. The size of the collector region is larger than the other two regions because it collects the charge carriers from the base.

Schematic representation and symbols of *n-p-n* and *p-n-p* is as shown below.



Biasing of Transistor

It is defined as the process of applying external voltages or potential difference to it. The biasing of the two *p-n* junction transistors, *i.e.* **emitter junction** and **collector junction** depends on the four modes. *i.e.* active mode, saturation mode, cut-off mode and inverse mode.

(i) **Active mode** is also known as *linear mode operation*. In this, emitter-base junction is forward biased and collector-base junction is reverse biased.

(ii) In **saturation mode**, maximum collector current flows and transistor acts as a closed switch from collector to emitter terminal.

(iii) In **cut-off mode**, the circuit behaves as open switch where only leakage current flows.

(iv) The emitter and collector are interchanged in **inverse mode**.

Different modes of operation of a transistor is given below.

Operating mode	Emitter-base bias	Collector-base bias
Active	Forward	Reverse
Saturation	Forward	Forward
Cut off	Reverse	Reverse
Inverse	Reverse	Forward

Note In *p-n-p* and *n-p-n* transistors,

Emitter current = Base current + Collector current

Transistor Circuit Configurations

In a transistor, one terminal out of the three serves as a reference point for the entire circuit. This terminal should be common to the input and output circuits and is connected to the ground. So, a transistor can be used in the following three configurations.

(i) Common Emitter (CE) Configuration

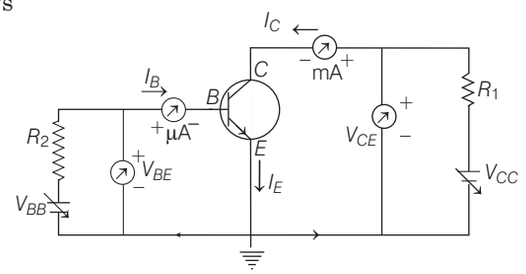
(ii) Common Base (CB) Configuration

(iii) Common Collector (CC) Configuration

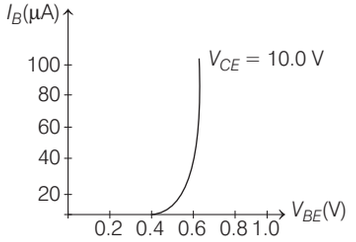
Common Emitter Characteristics

The graphs drawn between voltages and currents, when emitter of a transistor is common to input and output circuits are known as CE characteristics of a transistor.

The circuit of *n-p-n* transistor in CE configuration is as follows



Input Characteristics It represents the variation of base current I_B with the base-emitter voltage V_{BE}. It is as shown below



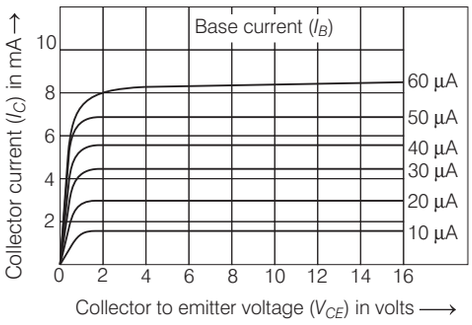
Here, increase in V_{CE} appear as increase in V_{CB}, its effect on I_B is negligible. As a consequence, input characteristics for various values of V_{CE} will give identical curves.

Hence, it is enough to determine only one input characteristics.

Input resistance is reciprocal of slope of I_B-V_{BE} curve.

Input resistance, $R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$

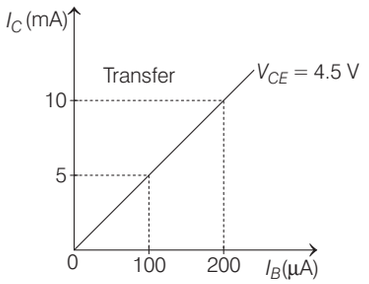
Output Characteristics It represents variation of the collector current I_C with the collector-emitter voltage V_{CE}. It is as shown below.



Output resistance, $r_o = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\text{ = constant}}$

= Reciprocal of slope of I_C-V_{CE} curve

Transfer Characteristics It is the graph between the collector current I_C and the base current I_B at constant values of collector-emitter voltage V_{CE}.



Current Amplification Factor

Current amplification factor β of a transistor in CE configuration is given by $\beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$

Its value is very large ($\beta_{AC} >> 1$).

In case of common base configuration,

It is the ratio of small change in the collector current to the small change in the emitter current at constant collector-base voltage. It is denoted by α and is given by

$$\alpha = \left[\frac{\Delta I_C}{\Delta I_E}\right]_{V_{CB}\text{ = constant}}$$

Relation between α and β

The relation between α and β can be given as follows

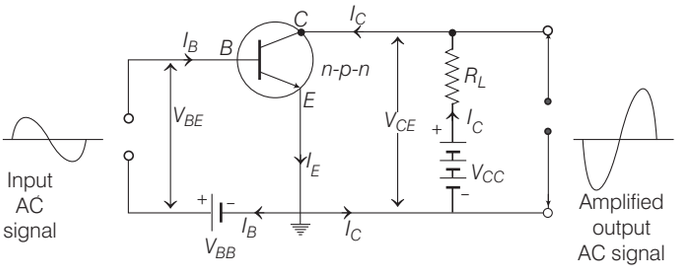
$$\alpha = \frac{\beta}{1+\beta} \quad \text{and} \quad \beta = \frac{\alpha}{1-\alpha}$$

Note α and β are independent of current, if the emitter-base junction is forward biased and the collector-base junction is reverse biased.

Transistor as an Amplifier

An amplifier is a device which is used for increasing the strength of amplitude of input signal. A transistor can be used for amplifying a weak signal. For a transistor to be operated as amplifier, in any of the configurations namely common base, common emitter and common collector.

The circuit diagram for *n-p-n* transistor as common emitter amplifier is shown in the figure given below.



From the above circuit, we get

$$I_E = I_B + I_C \text{ and } V_{CE} = V_{CC} - I_C R_L$$

Resistance gain The ratio of output (load) resistance to the input resistance is called resistance gain.

$$\therefore \quad \text{Resistance gain} = \frac{R_{\text{out}}}{R_{\text{in}}}$$

Voltage gain The ratio of change in output voltage to the change in input voltage is called voltage gain. It is denoted by A_V.

$$\text{Voltage gain,} \quad A_V = \frac{\Delta V_C}{\Delta V_b} = \frac{\Delta i_C}{\Delta i_B} \times \frac{R_{\text{out}}}{R_{\text{in}}}$$

$$\Rightarrow \quad A_V = \beta \times \text{resistance gain}$$

Power gain The ratio of change in output power to the change in input power is called power gain.

$$\therefore \quad \text{Power gain} = \frac{P_{\text{out}}}{P_{\text{in}}}$$

Also, power gain = $\beta^2 \times$ resistance gain

Transconductance (g_m)

It is defined as the ratio of the change in the collector current to the change in the base-to-emitter voltage at constant collector-to-emitter voltage and is denoted by g_m.

$$\text{Thus,} \quad g_m = \left(\frac{\Delta I_C}{\Delta V_{BE}}\right)_{V_{CE}} \quad \text{or} \quad g_m = \frac{\beta_{AC}}{R_{\text{in}}}$$

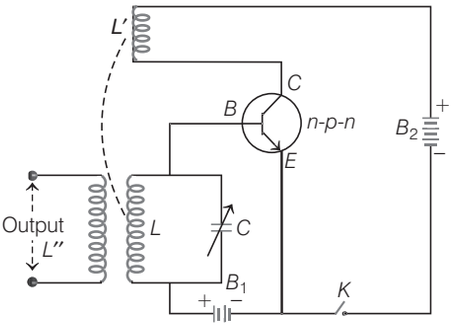
The unit of g_m is Ω^{-1} (ohm^{-1}) or S (siemen).

Transistor as an Oscillator

Transistor can be used as an oscillator which produces electrical oscillation of constant frequency and amplitude without any external input signal.

External input is necessary to sustain AC signal in the output of an amplifier. In case of oscillator, an AC output is received without any external input signal.

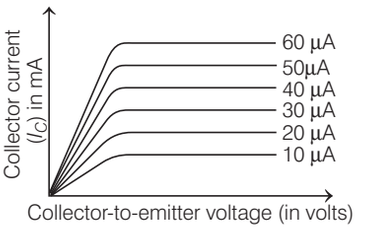
The feedback in the oscillators can be achieved by inductive coupling on *LC* or *RC* networks. The circuit used for an oscillator is an shown below.



The frequency of oscillations is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Example 9. *When a transistor is used in common emitter configuration, the following output characteristics are obtained. When V_{CE} is 10 V and I_C is 4 mA, then the value of β_{AC} (current amplification factor) is*



(a) 50 (b) 100 (c) 150 (d) 200

Sol. (c) Current amplification factor (β) is

$$\beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}}$$

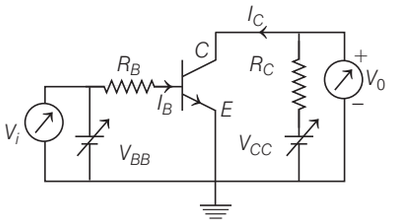
For finding the value of β_{AC} at the given values, take any two characteristics of I_B which lie above and below the given value of I_C. Here, I_C = 4 mA (choose characteristics for I_B = 30 μA and 20 μ A). At V_{CE} = 10 V, we read the two values of I_C from the graph, then

$$\Delta I_B = (30 - 20)\ \mu A = 10\ \mu A$$

$$\Delta I_C = (4.5 - 3)\ \text{mA} = 1.5\ \text{mA}$$

$$\therefore \quad \beta_{AC} = 1.5\ \text{mA}/10\ \mu A = 150$$

Example 10. *In the given figure, the V_{BB} supply can be varied from 0 V to 5V. The Si transistor has β_{DC} = 250, R_B = 100 k Ω, R_C = 1k Ω and V_{CC} = 5 V. Assume that, when the transistor is saturated, V_{CE} = 0 V and V_{BE} = 0.8 V. The minimum base current for which the transistor will reach saturation is*



(a) 10 μA (b) 20 μA (c) 30 μA (d) 40 μA

Sol. (b) At saturation, $V_{CE} = 0$ V

$$V_{BE} = 0.8 \text{ V}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{5 \text{ V}}{1 \text{k}\Omega} = 5 \text{ mA}$$

and $$I_B = \frac{I_C}{\beta} = \frac{5 \text{ mA}}{250} = 20 \text{ μA}$$

Example 11. *For a CE transistor amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100. The value of R_B in series with V_{BB} supply of 2V, if the DC base current has to be 10 times the signal current is* ***[NCERT]***

(a) 4 k Ω (b) 14 k Ω (c) 28 k Ω (d) 54 k Ω

Sol. (b) The output AC voltage is 2 V, so the AC collector current, $$I_c = \frac{2}{2000} = 1 \text{mA}$$

The signal current through the base is given by

$$I_B = \frac{I_c}{\beta} = \frac{1 \text{mA}}{100} = 0.010 \text{ mA}$$

The DC base current has to be $10 \times 0.010 = 0.10$ mA

$$\therefore \quad R_B = \frac{(V_{BB} - V_{BE})}{I_B}, V_{BE} = 0.6 \text{ V}$$

$$\therefore \quad R_B = \frac{(2 - 0.6)}{0.10} = 14 \text{ k } \Omega$$

Example 12. *In a CE transistor amplifier, the output resistance in 500 kΩ and current gain β = 49. If the power gain of the amplifier is 5×10^6, the input resistance is*

(a) 240 Ω (b) 165 Ω (c) 180 Ω (d) 290 Ω

Sol. (a) Given, 500 kΩ, β = 49 and $P = 5 \times 10^6$

We have, $$P = \beta^2 \frac{R_o}{R_i}$$

$$5 \times 10^6 = \frac{(49)^2 \times 500 \times 10^3}{R_i}$$

$$\therefore \quad R_i = \frac{49 \times 49 \times 500 \times 10^3}{5 \times 10^6} = 240 \text{ Ω}$$

Example 13. *An n-p-n transistor is used in common emitter configuration as an amplifier with 1 kΩ load resistance. Signal voltage of 10 mV is applied across the base-emitter. This produces a 3 mA change in the collector current and 15 μA change in the base current of the amplifier. The input resistance and voltage gain are* ***[JEE Main 2019]***

(a) 0.67 kΩ, 200 (b) 0.33 kΩ, 1.5
(c) 0.67 kΩ, 300 (d) 0.33 kΩ, 300

Sol. (c) Given, load resistance, $R_L = 1 \text{k}\Omega$

Input voltage, $V_{\text{in}} = 10 \text{ mV} = 10 \times 10^{-3}$ V

Base current, $\Delta I_B = 15 \text{ μA} = 15 \times 10^{-6}$ A

Collector current, $\Delta I_C = 3$ mA

Input resistance, $$R_{\text{in}} = \frac{V_{\text{in}}}{\Delta I_B} = \frac{10 \times 10^{-3}}{15 \times 10^{-6}} = 0.67 \text{k}\Omega$$

and voltage gain $$= \beta \times \frac{R_L}{R_{\text{in}}} = \frac{\Delta I_C \times R_L}{\Delta I_B \times R_{\text{in}}}$$

$$= \left(\frac{3 \text{ mA}}{15 \text{ μA}}\right) \times \left(\frac{1 \text{k}\Omega}{0.67 \text{ k}\Omega}\right)$$

$$= \left(\frac{3 \times 10^{-3}}{15 \times 10^{-6}}\right)\left(\frac{1 \times 10^3}{0.67 \times 10^3}\right)$$

$$= \frac{1000 \times 3 \times 3}{15 \times 2} = 300 \qquad (\because 0.67 \cong 2/3)$$

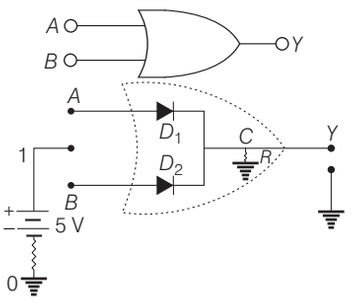
Logic Gates

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions, i.e. low (0) or high (1), represented by different voltage levels.

The basic logic gates are of three types

OR Gate

It is a device which has two or more inputs and one output. The logic symbol of OR gate is



Realisation of OR gate using two *p-n* junction diodes

The Boolean expression for OR gate is $Y = A + B$

This indicates Y equals A OR B.

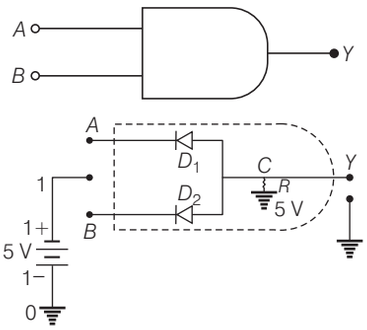
Truth table for OR gate ($Y = A + B$)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

The output of an OR gate assumes 1, if one or more inputs assume 1. The output is high when either of inputs A or B is high, but not if both A and B are low.

AND Gate

It is a device which has also two or more inputs and one output. The logic symbol of AND gate is given as



Realisation of an AND gate

The Boolean expression is $Y = A \cdot B$. This indicates Y equals to A AND B.

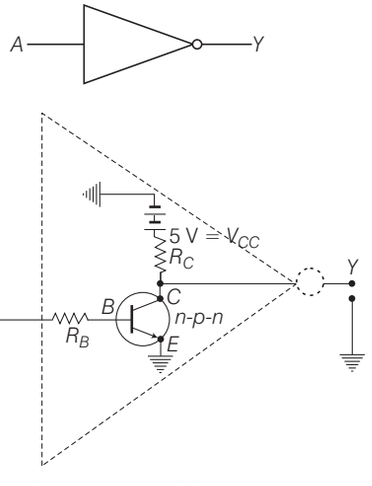
Truth table for AND gate ($Y = A \cdot B$)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

The output of an AND gate is 1 only, when all the inputs assume 1.

NOT Gate

It is a device which has only one input and only one output. The logic symbol of NOT gate is as shown in the following figure.



Realisation of NOT gate

The Boolean expression for NOT gate is $Y = \overline{A}$, which indicates Y equals NOT A.

Truth Table for NOT gate ($Y = \overline{A}$)

A	Y
0	1
1	0

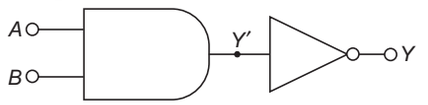
The output of a NOT gate assumes 1, if input is 0 and *vice-versa*.

Combination of Logic Gates

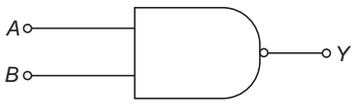
Few combinations of basic gates are given below

NAND Gate

In this type of gate, the output of AND gate is fed to input of a NOT gate and final output is obtained at output of NOT gate.



The logic symbol of NAND gate is shown as



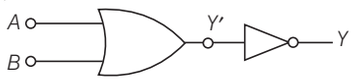
The Boolean expression of NAND gate is $Y = \overline{A \cdot B}$, which indicates A and B are negated.

Truth table for NAND gate

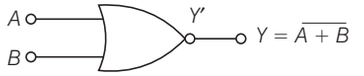
A	B	Y'	Y
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

NOR Gate

In this type of gate, the output of OR gate is fed to input of the NOT gate and final output is obtained at output of the NOT gate.



The logic symbol of NOR gate is shown as



The Boolean expression for NOR gate is $Y = \overline{A + B}$, which indicates that A OR B are negated.

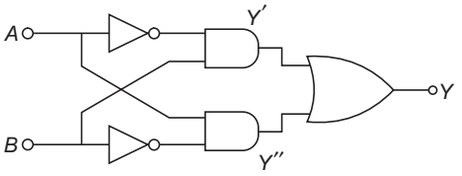
Truth table for NOR gate

A	B	Y'	Y
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

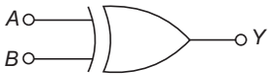
The NOR gate and NAND gate can be said to be **universal gates,** since combinations of them can be used to accomplish any of the basic operations and can thus produce an inverter, an OR gate or an AND gate.

XOR Gate

The XOR gate can be obtained by the combination of OR, AND and NOT gates as shown below.



The logic symbol of XOR gate is shown as



The Boolean expression for XOR gate is

$$Y = A\overline{B} + \overline{A}B = A \oplus B$$

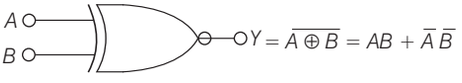
Truth Table for XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

From truth table, we can conclude that if A and B are not indentical, output is 1 and when A and B are indentical, output is 0.

XNOR Gate (exclusive-NOR) Gate

If XOR gate is combined with NOT gate, we get XNOR gate, *i.e.* the XOR gate followed by an inverter. Its output is "true" if the inputs are the same, and "false" if the inputs are different.



XNOR gate

Truth table for XNOR gate

Inputs		Output
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

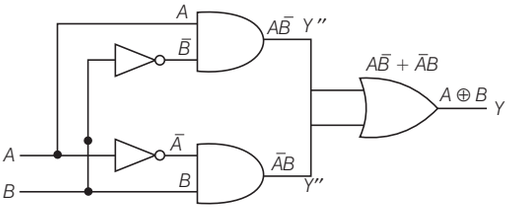
Some Useful Boolean Identities

- **Commutative laws**
  (i) $A + B = B + A$; (ii) $A \cdot B = B \cdot A$
- **Associative laws**
  (i) $A + (B + C) = (A + B) + C$;
  (ii) $A \cdot (B \cdot C) = (A + B) \cdot C$
- **Distributive laws**
  (i) $A \cdot (B + C) = A \cdot B + A \cdot C$;
  (ii) $(A + B) \cdot (A + C) = A + B \cdot C$
- **Absorption laws**
  (i) $A + A \cdot B = A$; (ii) $A \cdot (A + B) = A$;
  (iii) $\overline{A} \cdot (A + B) = \overline{A} \cdot B$
- **Double complement function**
  $\overline{\overline{A}} = A$, $\overline{\overline{A + B}} = A + B$; $\overline{\overline{A.B}} = A \cdot B$
- **Boolean indentities**
  (i) $A \cdot (\overline{A} + B) = A \cdot B$
  (ii) $A + \overline{A} \cdot B = A + B$
  (iii) $A + B \cdot C = (A + B) \cdot (A + C)$
  (iv) $(\overline{A} + B) \cdot (A + C) = \overline{A} \cdot C + A \cdot B$
- **De-Morgan's Theorem** It states that the complement of the whole sum is equal to the product of individual complements and *vice-versa. i.e.*
  (i) $\overline{A + B} = \overline{A} \cdot \overline{B}$ (ii) $\overline{A \cdot B} = \overline{A} + \overline{B}$
- **Basic OR and AND relations**

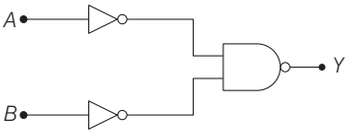
	OR	**AND**
(i)	$A + 0 = A$	$A \cdot 0 = 0$
(ii)	$A + 1 = 1$	$A \cdot 1 = A$
(iii)	$A = A = A$	$A \cdot A = A$
(iv)	$A + \overline{A} = 1$	
	$A \cdot \overline{A} = 0$	

- $A \oplus B = A\overline{B} + B\overline{A}$ (A AND NOT B OR B AND NOT A).
- $A \oplus B = (A + B)(\overline{AB})$ (A OR B AND NOT A AND B).

  It can be implemented by the gate arrangements as shown below.

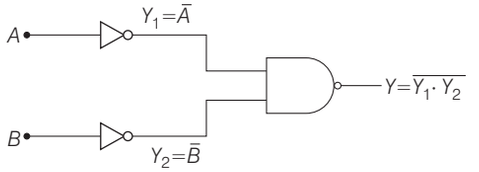


Example 14. *The logic gate equivalent to the given logic circuit is* **[JEE Main 2019]**



(a) NOR *(b)* NAND *(c)* OR *(d)* AND

Sol. (c) The given logic gate circuit can be drawn as shown below



Here, $Y=\overline{Y_1\cdot Y_2}=\overline{\overline{A}\cdot\overline{B}}$

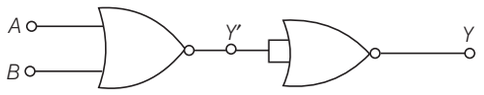
Using de-Morgan's theorem, *i.e.*

$$\overline{x\cdot y}=\overline{x}+\overline{y}$$

$\therefore$ $Y=\overline{\overline{A}}+\overline{\overline{B}}=A+B$ $[\because \overline{\overline{x}}=x]$

This represents the boolean expression for OR gate.

Example 15. *In the following circuit, the output* 1 *for all possible inputs A and B is expressed by which of the truth table given below*



(*a*)

A	*B*	*Y*
0	0	0
0	1	1
1	0	1
1	1	1

(*b*)

A	*B*	*Y*
0	0	1
0	1	0
1	0	1
1	0	1

(*c*)

A	*B*	*Y*
0	0	0
0	1	1
1	1	1
1	1	1

(*d*)

A	*B*	*Y*
1	1	1
0	1	0
1	1	0
0	1	1

Sol. (a) **Boolean expression**

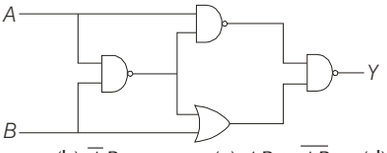
$$Y'=\overline{A+B}$$

and $Y=\overline{Y}=\overline{\overline{A+B}}=A+B$

Truth Table

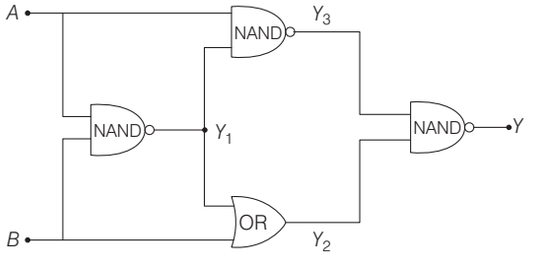
A	*B*	*Y'*	$\overline{Y'}=Y$
0	0	1	0
1	0	0	1
0	1	0	1
1	1	0	1

Example 16. *The output of the given logic circuit is* ***[JEE Main 2019]***

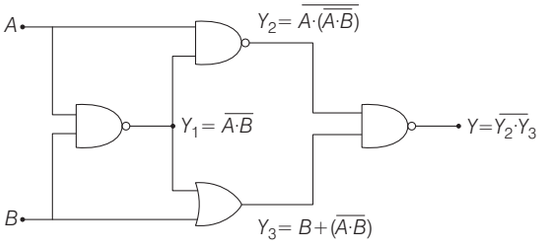


(a) $A\overline{B}$ (b) $\overline{A}B$ (c) $AB+\overline{A}\overline{B}$ (d) $A\overline{B}+\overline{A}B$

Sol. (*a*) Truth table for given circuit is



Using Boolean algebra, output of the given logic circuit can be given as



Here $Y_2=\overline{A\cdot(\overline{A\cdot B})}$

Using de-Morgan's principle,

$$\overline{x\cdot y}=\overline{x}+\overline{y} \text{ and } \overline{x+y}=\overline{x}\cdot\overline{y}$$

$\Rightarrow$ $Y_2=\overline{A}+(\overline{\overline{A\cdot B}})$ $[\because \overline{\overline{x}}=x]$

$=\overline{A}+(A\cdot B)$ ...(i)

Similarly, $Y_3=B+\overline{A}+\overline{B}=1+\overline{A}$ $[\because x+\overline{x}=1]$

$\Rightarrow$ $Y_3=1$ ...(ii) $[\because \overline{x}+1=1]$

As, $Y=\overline{Y_2\cdot Y_3}$

Using Eqs. (i) and (ii), we get

$Y=(\overline{\overline{A}+A\cdot B})(1)$

$=(\overline{\overline{A}+A\cdot B})+\overline{1}=\overline{\overline{A}}\cdot(\overline{A\cdot B})+0$

$=A\cdot(\overline{A}+\overline{B})$ $[\because x+0=x]$

$=A\cdot\overline{A}+A\cdot\overline{B}$ $[\because x\overline{x}=0]$

$=A\overline{B}$

Practice Exercise

ROUND I Topically Divided Problems

Semiconductors

1. The forbidden energy band gap in conductors, semiconductors and insulators are EG_1, EG_2 and EG_3, respectively. The relation among them, is **[NCERT]**

(a) $EG_1 < EG_2 < EG_3$ (b) $EG_1 > EG_2 > EG_3$
(c) $EG_2 > EG_1 < EG_3$ (d) $EG_3 > EG_1 > EG_2$

2. Hole is **[NCERT Exemplar]**

(a) an anti-particle of electron
(b) a vacancy created when an electron leaves a covalent bond
(c) absence of free electrons
(d) an artifically created particle

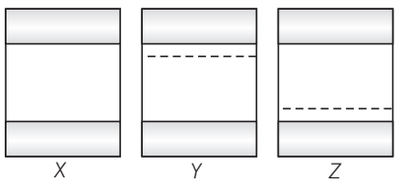
3. In an *n*-type semiconductor, which of the following statements is true? **[NCERT]**

(a) Electrons are majority carriers and trivalent atoms are the dopants.
(b) Electrons are minority carriers and pentavalent atoms are the dopants.
(c) Holes are minority carriers and pentavalent atoms are the dopants.
(d) Holes are majority carriers and trivalent atoms are the dopants.

4. The conductivity of a semiconductor increases with increase in temperature because **[NCERT Exemplar]**

(a) number density of free current carriers increases
(b) relaxation time increases
(c) Both number density of carriers and relaxation time increase
(d) number density of carriers increases, relaxation time decreases but effect of decreases in relaxation time is much less than increase in number density

5. The energy band diagrams for three semiconductor samples of silicon are as shown. We can then assert that,



(a) sample *X* is undoped while samples *Y* and *Z* have been doped with a third group impurity respectively
(b) sample *X* is undoped while both samples *Y* and *Z* have been doped with a fifth group impurity
(c) sample *X* has been doped with equal amounts of third and fifth group impurities while samples *Y* and *Z* are undoped
(d) sample *X* is undoped while samples *Y* and *Z* have been doped with a fifth group and a third group impurity respectively

6. The ratio of electron and hole current in a semiconductor is 7/4 and the ratio of drift velocities of electrons and holes is 5/4, then ratio of concentrations of electrons and holes will be

(a) 5/7 (b) 7/5
(c) 25/49 (d) 49/25

7. Mobility of electrons in a semiconductor is defined as the ratio of their drift velocity to the applied electric field. If for an *n*-type semiconductor, the density of electrons is 10^{19} m^{-3} and their mobility is 1.6 m^2 /V-s, then the resistivity of the semiconductor (since, it is an *n*-type semiconductor contribution of holes is ignored) is close to **[JEE Main 2019]**

(a) 2 Ω-m (b) 0.2 Ω-m
(c) 0.4 Ω-m (d) 4 Ω-m

8. A silicon specimen is made into a *p*-type semiconductor by doping, on an average, one indium atom per 5×10^7 silicon atoms. If the number density of atoms in the silicon specimen is 5×10^{28} atoms m^{-3}, then the number of acceptor atoms in silicon per cubic centimetre will be

(a) 2.5×10^{30}
(b) 2.5×10^{35}
(c) 1.0×10^{13}
(d) 1.0×10^{15}

9. The length of germanium rod is 0.928 cm and its area of cross-section is 1 mm^2. If for germanium $n_i = 2.5 \times 10^{19}$ m^{-3}, $\mu_h = 0.19$ $m^2V^{-1}s^{-1}$ $\mu_e = 0.39$ $m^2V^{-1}s^{-1}$, then its resistance will be

(a) 2.5 kΩ (b) 4.0 kΩ (c) 5.0 kΩ (d) 10.0 kΩ

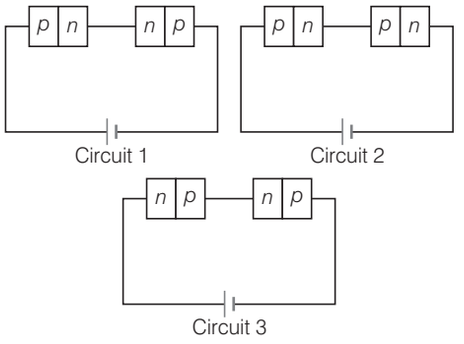
10. A pure germanium plate of area 3.5×10^{-4} m^2 and of thickness 1.5×10^{-3} m is connected across a battery of potential 5 V. Find the amount of heat generated in the plate in 120 s. Given that, the concentration of carriers in germanium at room temperature is 1.6×10^{6} per cubic metre. The mobilities of electrons and holes are $0.4\ m^2 V^{-1}\ s^{-1}$ and $0.2\ m^2\ V^{-1}\ s^{-1}$, respectively.

(a) 10.74×10^{-11} (b) 9×10^{-6}

(c) 10.48×10^{-9} (d) 6.26×10^{-10}

Junction Diode

11. Two identical *p-n* junction may be connected in series with a battery in three ways as shown in the adjoining figure. The potential drop across the *p-n* junctions are equal in



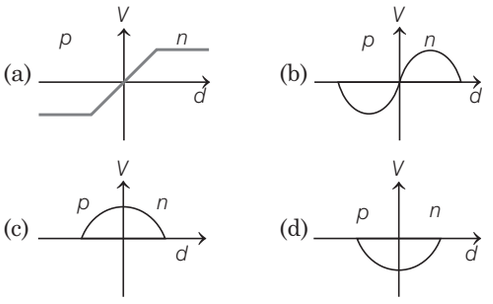
(a) circuit 1 and circuit 2

(b) circuit 2 and circuit 3

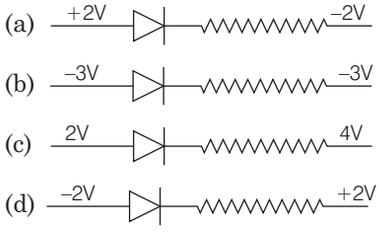
(c) circuit 3 and circuit 1

(d) circuit 1 only

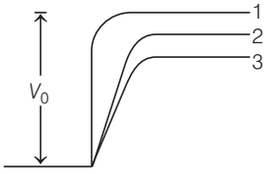
12. The correct curve between potential (V) and distance (d) near *p-n* junction is



13. The forward biased diode connection is **[JEE Main 2014]**



14. In figure, V_0 is the potential barrier across a *p-n* junction, when no battery is connected across the junction **[NCERT Exemplar]**



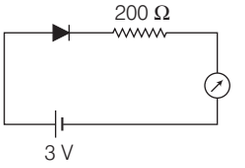
(a) 1 and 3 both correspond to forward bias of junction

(b) 3 corresponds to forward bias of junction and 1 corresponds to reverse bias of junction

(c) 1 corresponds to forward bias and 3 corresponds to reverse bias of junction

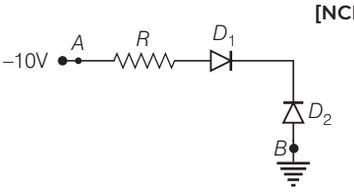
(d) 3 and 1 both correspond to reverse bias of junction

15. The reading of the ammeter for a silicon diode in the given circuit is **[JEE Main 2018]**



(a) 0 (b) 15 mA (c) 11.5 mA (d) 13.5 mA

16. In figure assuming the diodes to be ideal, **[NCERT Exemplar]**



(a) D_1 is forward biased and D_2 is reverse biased and hence current flows from A to B

(b) D_2 is forward biased and D_1 is reverse biased and hence no current flows from B and A and *vice-versa*

(c) D_1 and D_2 are both forward biased and hence current flows from A to B

(d) D_1 and D_2 are both reverse biased and hence no current flows from A to B and *vice-versa*

17. The reverse bias in a junction diode is changed from 8 V to 13 V, then the value of the current changes from 40 μ A to 60 μA. The resistance of junction diode will be

(a) $2 \times 10^5\ \Omega$ (b) $2.5 \times 10^5\ \Omega$

(c) $3 \times 10^5\ \Omega$ (d) $4 \times 10^5\ \Omega$

18. The breakdown in a reverse biased *p-n* junction diode is more likely to occur due to

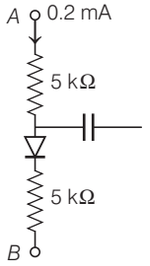
(a) large velocity of the minority charge carriers, if the doping concentration is small

(b) large velocity of the minority charge carriers, if the doping concentration is large

(c) strong electric field in a depletion region, if the doping concentration is small

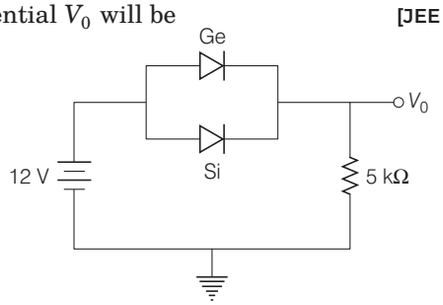
(d) Both (a) and (c)

19. In the circuit shown in figure. If the diode forward voltage drop is 0.3 V, the voltage difference between A and B is **[NCERT Exemplar]**



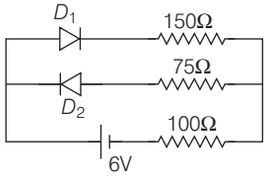
(a) 1.3 V (b) 2.3 V (c) 0 (d) 0.5 V

20. At 0.3 V and 0.7 V, the diodes Ge and Si become conductor respectively. In given figure, if ends of diode Ge overturned, the change in potential V_0 will be **[JEE Main 2019]**



(a) 0.2 V (b) 0.6V (c) 0.4 V (d) 0.8V

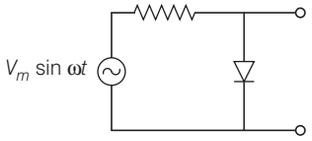
21. The circuit shown below contains two ideal diodes, each with a forward resistance of 50 Ω. If the battery voltage is 6 V, the current through the 100 Ω resistance (in ampere) is **[JEE Main 2019]**



(a) 0.027 (b) 0.020 (c) 0.030 (d) 0.036

Rectifier and Special Purpose Diode

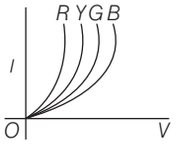
22. The output of the given circuit in figure **[NCERT Exemplar]**

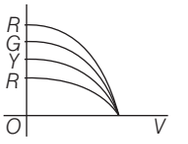


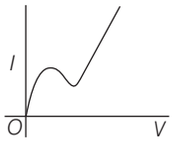
(a) would be zero at all times
(b) would be like a half-wave rectifier with positive cycle in output
(c) would be like a half-wave rectifier with negative cycle in output
(d) would be like that of a full wave rectifier

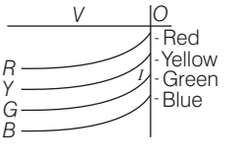
23. A semiconductor diode is used as a half wave rectifier having internal resistance 200 Ω. The voltage applied is given by $V = (50 \sin \omega t)$ volt and load resistance is 650 Ω. Then
(a) maximum output current is 58 mA
(b) DC output current is 18.5 mA
(c) DC output power is 0.22 W
(d) All of the above

24. The I-V characteristic of an LED is **[JEE Main 2013]**

(a) 

(b) 

(c) 

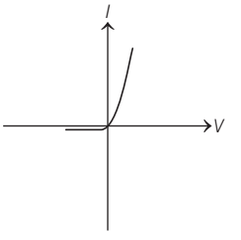
(d) 

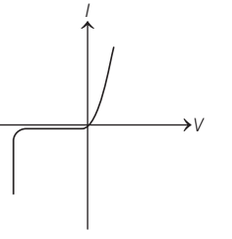
25. If a semiconductor photodiode can detect a photon with a maximum wavelength of 400 nm, then its band gap energy is
(Take, Planck's constant, $h = 6.63 \times 10^{-34}$ J-s and speed of light, $c = 3 \times 10^8$ m/s) **[JEE Main 2020]**
(a) 1.5 eV (b) 1.1 eV
(c) 3.1 eV (d) 2.0 eV

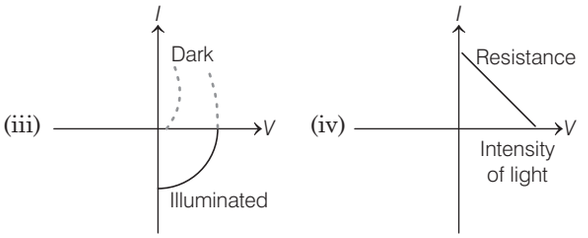
26. With increasing biasing voltage of a photodiode, the photocurrent magnitude **[JEE Main 2020]**
(a) increases initially and after attaining certain value, it decreases
(b) increases initially and saturates finally
(c) remains constant
(d) increases linearly

27. Three photodiodes D_1, D_2 and D_3 are made of semiconductors having band gaps of 2.5 eV, 2 eV and 3 eV, respectively. Which one will be able to detect light of wavelength of 6000 Å?
(a) D_1 (b) D_2
(c) D_3 (d) Both D_1 and D_2

28. Identify the semiconductor devices whose characteristics are as given below, in the order (i), (ii), (iii) and (iv).

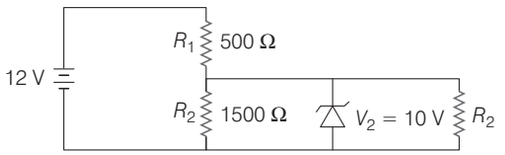
(i) 

(ii) 



(a) Simple diode, Zener diode, Solar cell, Light dependent resistance
(b) Zener diode, Simple diode, Light dependent resistance, Solar cell
(c) Solar cell, Light dependent resistance, Zener diode, Simple diode
(d) Zener diode, Solar cell, Simple diode, Light dependent resistance

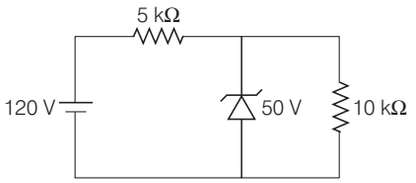
29. In the given circuit, the current through Zener diode is close to



[JEE Main 2019]

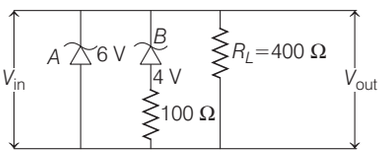
(a) 6.0 mA
(b) 6.7 mA
(c) 0
(d) 4.0 mA

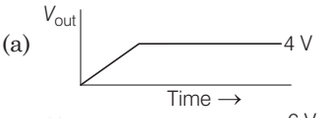
30. For the circuit shown below, the current through the Zener diode is **[JEE Main 2019]**

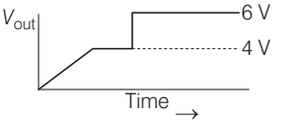


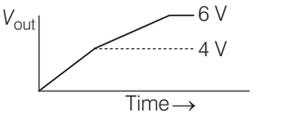
(a) 14 mA
(b) zero
(c) 5 mA
(d) 9 mA

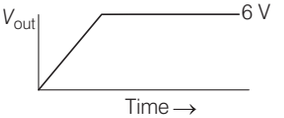
31. Two Zener diodes A and B having breakdown voltages of 6 V and 4 V respectively, are connected as shown in the circuit below. The output voltage V_{out} variation with input voltage linearly increasing with time, is given by ($V_{in} = 0$ V at $t = 0$) (figures are qualitative) **[JEE Main 2020]**



(a) 

(b) 

(c) 

(d) 

Junction Transistor

32. Consider an n-p-n transistor with its base-emitter junction forward biased and collector-base junction reverse biased. Which of the following statements are true?
(a) Electrons crossover from emitter-to-collector.
(b) Holes move from base-to-collector.
(c) Electrons from emitter move out of base without of base without of base without going to the collector
(d) Both (a) and (c)

33. The current gain of a transistor in a common emitter configuration is 40. If the emitter current is 8.2 mA, then base current is
(a) 0.02 mA (b) 0.2 mA (c) 2.0 mA (d) 0.4 mA

34. In a common emitter amplifier circuit using an n-p-n transistor, the phase difference between the input and the output voltages will be **[JEE Main 2017]**
(a) 90° (b) 135° (c) 180° (d) 45°

35. For a common-emitter configuration, if α and β have their usual meanings, the correct relationship between α and β is

(a) $\frac{1}{\alpha} = \frac{1}{\beta} + 2$ (b) $\alpha = \frac{\beta}{1-\beta}$

(c) $\alpha = \frac{\beta}{1+\beta}$ (d) $\alpha = \frac{\beta^2}{1+\beta^2}$

36. In an n-p-n transistor, the collector current is 10 mA, if 90% of the electrons emitted reach the collector, the emitter current I_E and base current I_B are given by
(a) $I_E = -1$ mA, $I_b = 9$ mA (b) $I_E = 9$ mA, $I_B = -1$ mA
(c) $I_E = 1$ mA, $I_B = 11$ mA (d) $I_E = 11$ mA, $I_B = 1$ mA

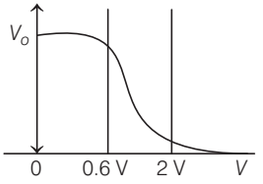
37. The transfer ratio of the transistor is 50. The input resistance of the transistor when used in the CE configuration is 1 kΩ. The peak value for an AC input voltage of 0.01 V of collector current is
(a) 500 μA (b) 0.25 mA (c) 400 mA (d) 0.01 mA

38. In a *n-p-n* transistor, 10^{10} electrons enter the emitter in 10^{-6} s and 4% of the electrons are lost in base. The current transfer ratio will be
(a) 0.98 (b) 0.97 (c) 0.96 (d) 0.94

39. The input signal given to a CE amplifier having a voltage gain of 150 is $V_i = 2\cos\left(15\,t + \frac{\pi}{3}\right)$. The corresponding output signal will be
(a) $300\cos\left(15t + \frac{\pi}{3}\right)$ (b) $75\cos\left(15t + \frac{2\pi}{3}\right)$
(c) $2\cos\left(15t + \frac{5\pi}{3}\right)$ (d) $300\cos\left(15t + \frac{4\pi}{3}\right)$

40. In a *n-p-n* transistor circuit, the collector current is 10 mA. If 95 per cent of the electrons emitted reach the collector, which of the following statements are true? **[NCERT Exemplar]**
(a) The emitter current will be 8 mA.
(b) The emitter current will be 10.53 mA.
(c) The base current will be 5.53 mA.
(d) The base current will be 2 mA.

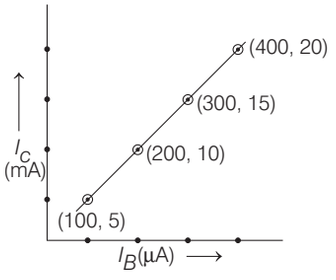
41. Figure shows the transfer characteristics of a base biased CE transistor. Which of the following statements are false?



(a) At V_i = 0.4 V, transistor is in active state.
(b) At V_i = 1 V, it can be used as an amplifier.
(c) At V_i = 0.5 V, It can be used as a switch turned OFF.
(d) At V_i = 2.5 V, it can be used as a switch turned ON.

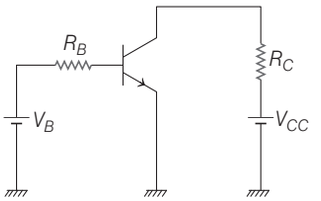
42. An *n-p-n* transistor operates as a common emitter amplifier, with a power gain of 60 dB. The input circuit resistance is 100 Ω and the output load resistance is 10 kΩ. The common emitter current gain β is **[JEE Main 2019]**
(a) 10^2 (b) 6×10^2 (c) 10^4 (d) 60

43. The transfer characteristic curve of a transistor, having input and output resistances 100 Ω and 100 kΩ respectively, is shown in the figure. The voltage and power gains are respectively **[JEE Main 2019]**



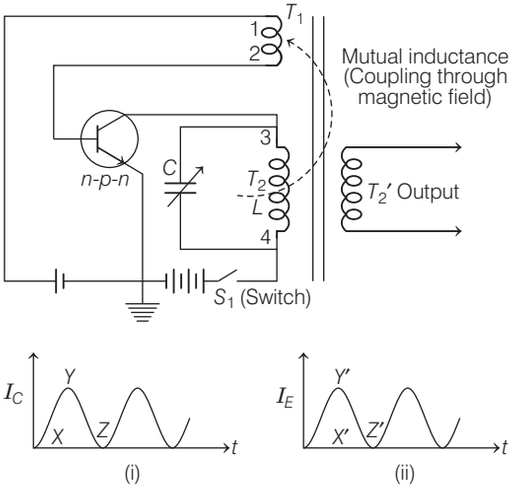
(a) $2.5\times10^4, 2.5\times10^6$
(b) $5\times10^4, 5\times10^6$
(c) $5\times10^4, 5\times10^5$
(d) $5\times10^4, 2.5\times10^6$

44. A common emitter amplifier circuit, built using an *n-p-n* transistor, is shown in the figure. Its DC current gain is 250, $R_C = 1\,\text{k}\Omega$ and $V_{CC} = 10$ V. What is the minimum base current for V_{CE} to reach saturation? **[JEE Main 2019]**



(a) 40 μA (b) 10 μA
(c) 100 μA (d) 7 μA

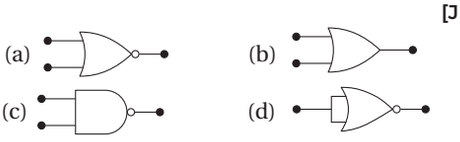
45. For tuned collector oscillator, using an *n-p-n* transistor its circuit diagram and rise & fall (or built up) of I_C, I_E current graphs, respectively are as shown below. Initially when switch S_1 is ON, it can be concluded



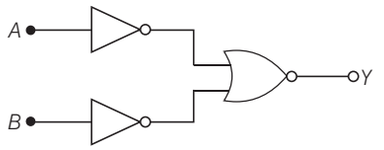
(a) Both I_C and I_E increase initially
(b) Both I_C and I_E decrease
(c) initially I_C increases but I_E decreases
(d) initially I_C decreases but I_E increases

Logic Gates

46. Which of the following gives a reversible operation? **[JEE Main 2020]**

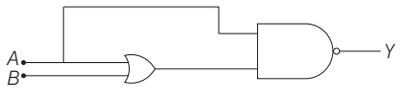


47. Which of the following logic gate is represented by the combination of logic gates?



(a) NAND gate (b) NOR gate
(c) AND gate (d) OR gate

48. The truth table for the circuit given in the figure is [JEE Main 2019]



(a)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	1

(b)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

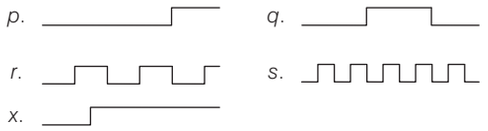
(c)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(d)

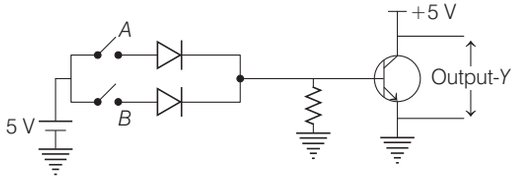
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

49. If p, q, r and s are inputs to a gate and x is its output, then as per the following time graph, the gate is



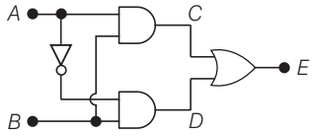
(a) NOT (b) AND (c) OR (d) NAND

50. Boolean relation at the output stage Y for the following circuit is [JEE Main 2020]



(a) $A \cdot B$ (b) $A + B$
(c) $\overline{A} + \overline{B}$ (d) $\overline{A} \cdot \overline{B}$

51. Truth table for the given circuit. [NCERT Exemplar]



(a)

A	B	E
0	0	1
0	1	0
1	0	1
1	1	0

(b)

A	B	E
0	0	1
0	1	0
1	0	0
1	1	1

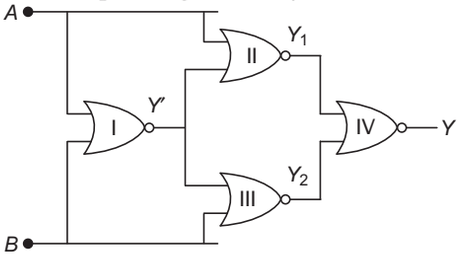
(c)

A	B	E
0	0	0
0	1	1
1	0	0
1	1	1

(d)

A	B	E
0	0	0
0	1	1
1	0	1
1	1	0

52. A system of four gates is set up as shown. The truth table corresponding to this system is [JEE Main 2013]



(a)

Inputs		Outputs
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(b)

Inputs		Outputs
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

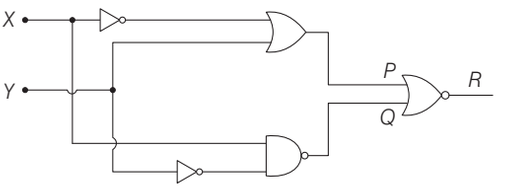
(c)

Inputs		Outputs
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(d)

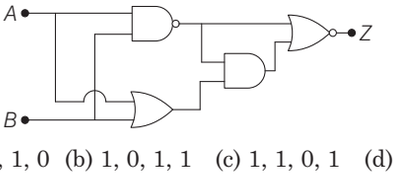
Inputs		Outputs
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

53. To get output 1 at R, for the given logic gate circuit, the input values must be [JEE Main 2019]



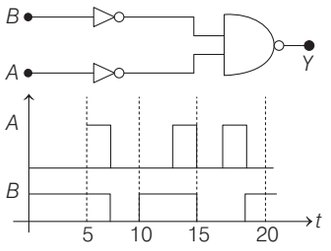
(a) $X = 0, Y = 0$ (b) $X = 1, Y = 0$
(c) $X = 1, Y = 1$ (d) $X = 0, Y = 1$

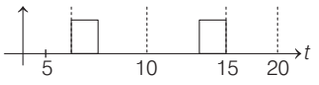
54. In the following digital circuit, what will be the output at Z, when the input (A, B) are (1, 0), (0, 0), (1, 1) and (0, 1)? [JEE Main 2020]

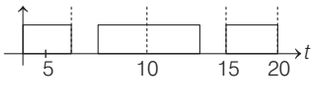


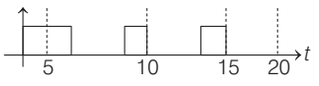
(a) 0, 0, 1, 0 (b) 1, 0, 1, 1 (c) 1, 1, 0, 1 (d) 0, 1, 0, 0

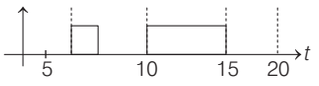
55. Identify the correct output signal Y in the given combination of gates (as shown) for the given inputs A and B. [JEE Main 2020]



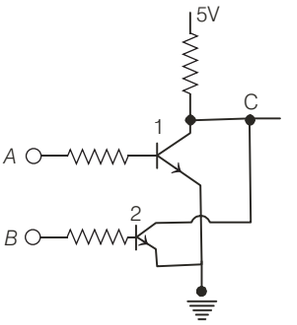
(a)


(b)


(c)


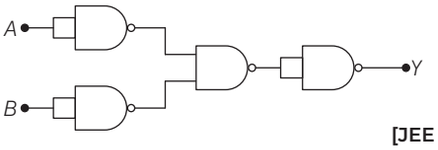
(d)


56. Consider two n-p-n transistors as shown in figure. If 0 V corresponds to false and 5 V corresponds to true, then the output at C corresponds to



(a) A NAND B (b) A OR B
(c) A AND B (d) A NOR B

57. The following logic gate is equivalent to



[JEE Main 2021]

(a) NOR gate (b) OR gate
(c) AND gate (d) NAND gate

ROUND II Mixed Bag

Only One Correct Option

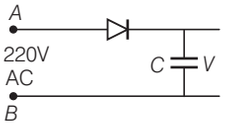
1. The output of an OR gate is connected to both the inputs of NAND gate. The combination will serve as a [IIT JEE 2011]

(a) OR gate (b) NOT gate
(c) NOR gate (d) AND gate

2. When A is the internal stage gain of an amplifier and β is the feedback ratio, then the amplitude becomes as oscillator if

(a) β is negative and magnitude of $\beta = \frac{A}{2}$
(b) β is negative and magnitude of $\beta = \frac{1}{A}$
(c) β is negative and magnitude of $\beta = A$
(d) β is positive and magnitude of $\beta = \frac{1}{A}$

3. A 220 V AC supply is connected between points A and B (figure). What will be the potential difference V across the capacitor? [NCERT Exemplar]



(a) 220 V (b) 110 V
(c) 0 V (d) $220\sqrt{2}$ V

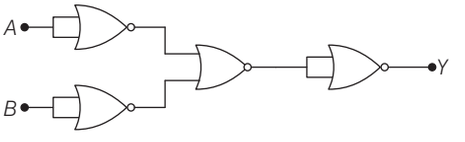
4. When a diode is forward biased, it has a voltage drop of 0.5 V. The safe limit of current through the diode is 10 mA. If a battery of emf 1.5 V is used in the circuit, the value of minimum resistance to be connected in series with the diode, so that the current does not exceed the safe limit is [JEE Main 2020]

(a) 300 Ω (b) 50 Ω (c) 100 Ω (d) 200 Ω

5. A Si and a Ge diode has identical physical dimensions and the band gap in Si is larger than that in Ge. An identical reverse bias is applied across the diodes, then [WB JEE 2008]

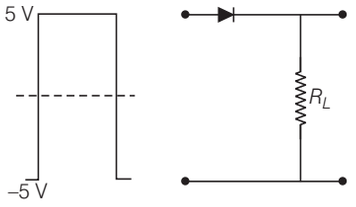
(a) the reverse current in Ge is larger than that in Si
(b) the reverse current in Si is larger than that in Ge
(c) the reverse current is identical in the two diodes
(d) the relative magnitude of the reverse currents cannot be determined from the given data only

6. The output of the given combination gates represents [JEE Main 2021]

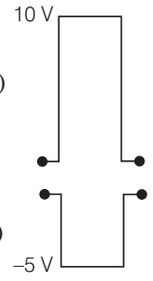


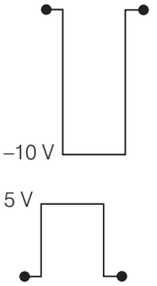
(a) XOR gate (b) NAND gate
(c) AND gate (d) NOR gate

7. If in a *p-n* junction diode, a square input signal of 10 V is applied as shown



Then the output signal across R_L will be **[AIEEE 2009]**

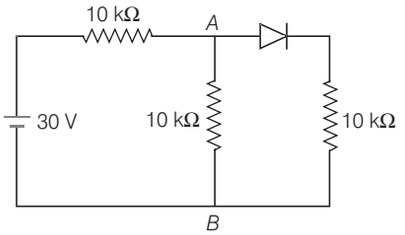
(a) 

(b) 

(c)

(d)

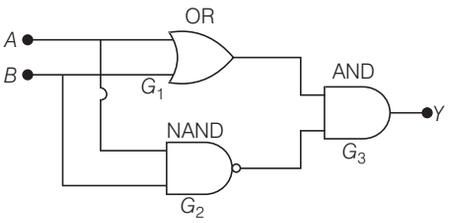
8. In the figure, potential difference between *A* and *B* is



(a) zero (b) 5 V
(c) 10 V (d) 15 V

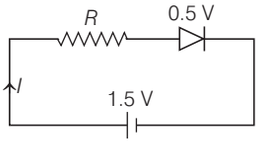
9. The input resistance of a common emitter transistor amplifier, if the output resistance is 500 kΩ, the current gain, $\alpha = 0.98$ and power gain is 6.0625×10^6, is
(a) 198 Ω
(b) 300 Ω
(c) 100 Ω
(d) 400 Ω

10. The following configuration of gate is equivalent to figure.



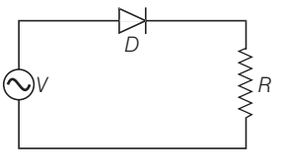
(a) NAND
(b) XOR
(c) OR
(d) None of the above

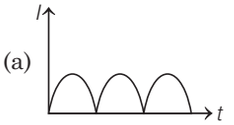
11. The diode used in the circuit shown in the figure has a constant voltage drop of 0.5 V at all currents and a maximum power rating of 100 mW. What should be the value of the resistor *R*, connected in series with the diode for obtaining maximum current ?

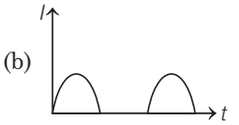


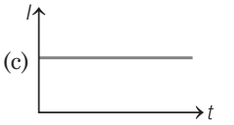
(a) 1.5 Ω (b) 5 Ω
(c) 6.67 Ω (d) 200 Ω

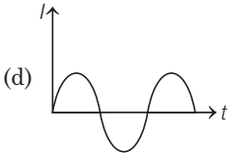
12. A *p-n* junction *D* shown in the figure can act as a rectifier. An alternating current source *V* is connected in the circuit. The current *I* in the resistor *R* can be shown by **[AIEEE 2009]**



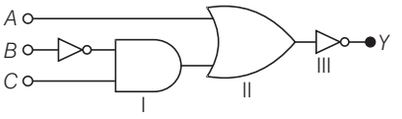
(a) 

(b) 

(c) 

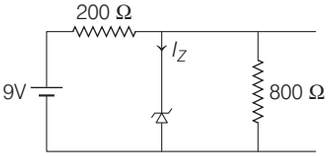
(d) 

13. The output *Y* of the logic circuit shown in figure is best represented as



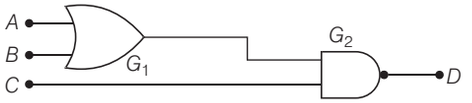
(a) $\overline{A} + \overline{A \cdot C}$ (b) $\overline{A + (\overline{B} \cdot C)}$
(c) $\overline{A + B \cdot C}$ (d) $\overline{A + \overline{B} + C}$

14. The reverse breakdown voltage of a Zener diode is 5.6 V in the given circuit. **[JEE Main 2019]**



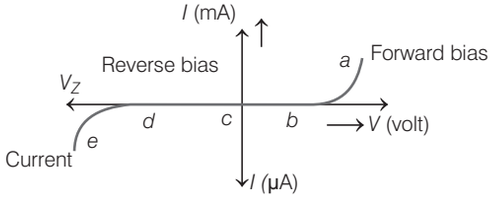
The current I_Z through the Zener is
(a) 10 mA (b) 17 mA
(c) 15 mA (d) 7 mA

15. For the given combination of gates, if the logic states of inputs A, B, C are as follows $A = B = C = 0$ and $A = B = 1, C = 0$, then the logic states of output D are



(a) 0, 0 (b) 0, 1 (c) 1, 0 (d) 1, 1

16. The graph given below represents the I-V characteristics of a Zener diode. Which part of the characteristics curve is most relevant for its operation as a voltage regulator? **[AMU Engg. 2009]**

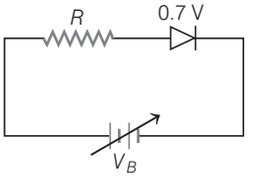


(a) ab (b) bc (c) cd (d) de

17. In a common emitter amplifier, using output resistance of 5000 Ω and input resistance of 2000 Ω, if the peak value of input signal voltage is 10 mV and $\beta = 50$, then peak value of output voltage is

(a) 5×10^{-6} V (b) 12.50×10^{-6} V
(c) 1.25 V (d) 125.0 V

18. The junction diode in the following circuit requires a minimum current of 1 mA to be above the knee point (0.7 V) of its I-V characteristic curve. The voltage across the junction diode is independent of current above the knee point, if $V_B = 4$ V, then the maximum value of R so that the voltage is above knee point will be



(a) 3.3 kΩ (b) 4.0 kΩ (c) 4.7 kΩ (d) 6.6 kΩ

19. **Statement I.** In a full wave rectifier circuit operating from 50 Hz mains frequency, the fundamental frequency in the ripple would be 100 Hz.

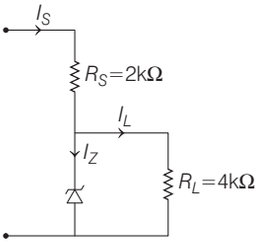
Statement II. In a semiconducting material, the mobilities of electron and hole are μ_e and μ_h respectively, then $\mu_e < \mu_h$.

Statement III. For an n-p-n transistor amplifier in CE configuration, the current gain in the transistor is 100. If the collector changes by 1 mA, then the change in emitter current is 1.01 mA.

Choose the correct statement and mark the correct option given below.

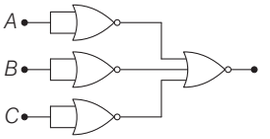
(a) Both I and II (b) Only II
(c) Both I and III (d) All of these

20. Figure shows a DC voltage regulator circuit, with a Zener diode of breakdown voltage = 6 V. If the unregulated input voltage varies between 10 V to 16 V, then what is the maximum Zener current? **[JEE Main 2019]**



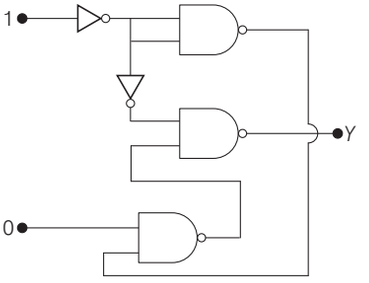
(a) 2.5 mA (b) 1.5 mA
(c) 7.5 mA (d) 3.5 mA

21. Identify the operation performed by the circuit given below. **[JEE Main 2020]**



(a) AND (b) NAND
(c) NOT (d) OR

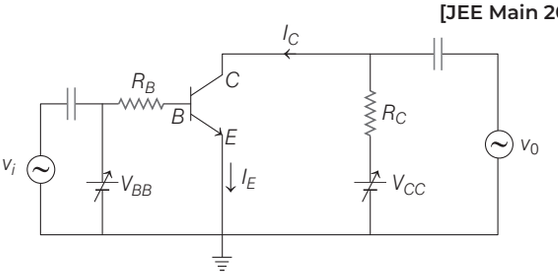
22. In the given circuit, value of Y is **[JEE Main 2020]**



(a) toggles between 0 and 1 (b) 1
(c) 0 (d) will not execute

23. In the figure, given that V_{BB} supply can vary from 0 to 5.0 V, $V_{CC} = 5$ V, $\beta_{DC} = 200$, $R_B = 100$ k Ω, $R_C = 1$ kΩ and $V_{BE} = 1.0$ V. The minimum base current and the input voltage at which the transistor will go to saturation, will be, respectively

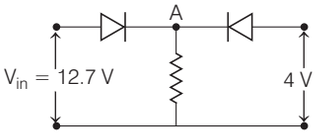
[JEE Main 2019]



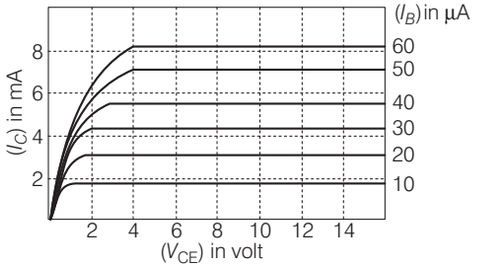
(a) 25 μA and 2.8 V (b) 25 μA and 3.5 V
(c) 20 μA and 3.5 V (d) 20 μA and 2.8 V

Numerical Value Questions

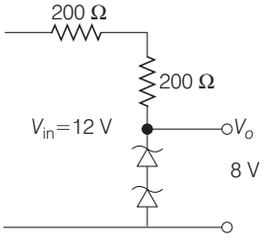
24. Both the diodes used in the circuit shown are assumed to be ideal and have negligible resistance when these are forward biased. Built in potential in each diode is 0.7V. For the input voltages shown in the figure, the voltage (in V) at point A is …… . **[JEE Main 2020]**



25. The output characteristics of a transistor is shown in the figure. When V_{CE} is 10V and I_C = 4.0 mA, then value of β_{AC} is …… . **[JEE Main 2020]**

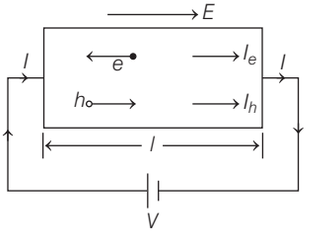


26. The circuit shown below is working as a 8 V DC regulated voltage source. When 12 V is used as input, the power dissipated (in mW) in each diode is (considering both Zener diodes are identical) ..... . **[JEE Main 2020]**



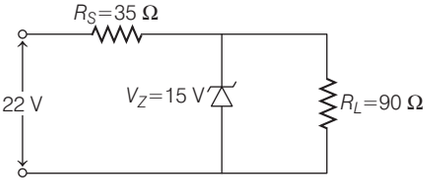
27. For a CE transister amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V Suppose the current amplification factor of the transistor is 100. Find the base current (in μA), if the base resistance is 1 kΩ.

28. In figure, a battery of emf 2V is used. The length of the block is 0.1 m and the area is $1 \times 10^4 m^2$. If the block is of intrinsic silicon at 300 K, find the electron and hole currents. The magnitude of the total current is $p \times 10^{-7}$ A , where the value of p is …… .



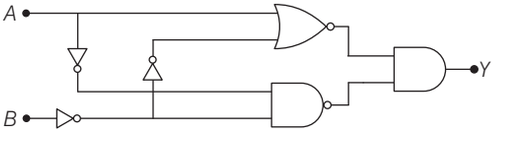
[Given for silicon, $n = 1.5 \times 10^{16}/m^3$, $\mu_e = 0.135\ m^2/V\text{-s}$, $\mu_h = 0.048 m^2/V\text{-s}$ and for germanium, $n = 2.4 \times 10^{19}/m^3$, $\mu_e = 0.39\ m^2/V\text{-s}$ and $\mu_h = 0.19\ m^2/V\text{-s}$]

29. The value of power dissipated across the zener diode (V_Z = 15 V) connected in the circuit as shown in figure is $x \times 10^{-1}$ watt.



The value of x, to the nearest integer, is …… . **[JEE Main 2021]**

30. In the logic circuit shown in the figure, if input A and B are 0 to 1 respectively, the output at Y would be 'x'. The value of x is …... . **[JEE Main 2021]**



Answers

Round I

1. *(a)*	***2.*** *(b)*	***3.*** *(c)*	***4.*** *(d)*	***5.*** *(d)*	***6.*** *(b)*	***7.*** *(c)*	***8.*** *(d)*	***9.*** *(b)*	***10.*** *(a)*
11. *(b)*	***12.*** *(a)*	***13.*** *(a)*	***14.*** *(b)*	***15.*** *(c)*	***16.*** *(b)*	***17.*** *(b)*	***18.*** *(b)*	***19.*** *(b)*	***20.*** *(c)*
21. *(b)*	***22.*** *(c)*	***23.*** *(d)*	***24.*** *(a)*	***25.*** *(c)*	***26.*** *(b)*	***27.*** *(b)*	***28.*** *(a)*	***29.*** *(c)*	***30.*** *(d)*
31. *(c)*	***32.*** *(a)*	***33.*** *(b)*	***34.*** *(c)*	***35.*** *(c)*	***36.*** *(d)*	***37.*** *(a)*	***38.*** *(c)*	***39.*** *(d)*	***40.*** *(b)*
41. *(a)*	***42.*** *(a)*	***43.*** *(d)*	***44.*** *(a)*	***45.*** *(a)*	***46.*** *(d)*	***47.*** *(c)*	***48.*** *(c)*	***49.*** *(c)*	***50.*** *(d)*
51. *(c)*	***52.*** *(a)*	***53.*** *(b)*	***54.*** *(a)*	***55.*** *(b)*	***56.*** *(c)*	***57.*** *(a)*			

Round II

1. *(c)*	***2.*** *(d)*	***3.*** *(d)*	***4.*** *(c)*	***5.*** *(c)*	***6.*** *(b)*	***7.*** *(c)*	***8.*** *(c)*	***9.*** *(d)*	***10.*** *(b)*
11. *(b)*	***12.*** *(b)*	***13.*** *(b)*	***14.*** *(a)*	***15.*** *(d)*	***16.*** *(d)*	***17.*** *(c)*	***18.*** *(a)*	***19.*** *(c)*	***20.*** *(d)*
21. *(a)*	***22.*** *(c)*	***23.*** *(b)*	***24.*** *12*	***25.*** *150*	***26.*** *40*	***27.*** *10*	***28.*** *8.784*	***29.*** *5*	***30.*** *0*

Solutions

Round I

1. In insulators, the forbidden energy gap is very large, in case of semiconductor, it is moderate and in conductors the energy-gap is zero.

Hence, $EG_1 < EG_2 < EG_3$.

2. Holes are formed when electrons in atoms move out of the valence band into the conduction band. In this situation, a vacancy is created in covalent band when electron leaves a covalent band, which is called a hole.

3. n-type semiconductor is obtained by doping the Ge or Si with pentavalent (dopants) atoms. In n-type semiconductor, electrons are majority carriers and holes are minority carriers.

4. On increasing the temperature of semiconductor, more number of covalent bonds break and large number of charge carriers are produced. Hence, number density of charge carriers increases. On increassing the temperature, relaxation time also decreases but effect of decrease in relaxation time is much less than increase in number density.

5. In sample X, no impurity energy level is seen, so it is undoped. In sample Y, impurity energy level lies below the conduction band, so it is doped with fifth group impurity. In sample Z, impurity energy level lies above the valence band, so it is doped with third group impurity.

6. As, $I = nAev_d$

or $I \propto nv_d$

$\therefore \quad \dfrac{I_e}{I_h} = \dfrac{n_e v_e}{n_h v_h}$ or $\dfrac{n_e}{n_h} = \dfrac{I_e}{I_h} \times \dfrac{v_h}{v_e} = \dfrac{7}{4} \times \dfrac{4}{5} = \dfrac{7}{5}$

7. Since, it is an n-type semiconductor and concentration of the holes has been ignored. So, its conductivity is given as $\sigma = n_e e \mu_e$, where n_e is the number density of electron, e is the charge on electron and μ_e is its mobility.

Substituting the given values, we get

$$\sigma = 10^{19} \times 1.6 \times 10^{-19} \times 1.6 = 2.56$$

As, resistivity, $\rho = \dfrac{1}{\sigma} = \dfrac{1}{2.56}$ or $\rho = 0.39 \simeq 0.4\ \Omega\text{-m}$

8. Number density of atoms in silicon specimen $= 5 \times 10^{28}$ atoms/m^2 $= 5 \times 10^7$ silicon atoms, so total number of indium atoms doped per cm^3 of silicon will be $n = 5 \times 10^{22}/5 \times 10^7 = 10^{15}$ atoms cm^{-3}.

9. We have, $R = \dfrac{\rho l}{A} = \dfrac{L}{n_i e(\mu_e + \mu_h)A}$

$$= \frac{0.928 \times 10^{-2}}{2.5 \times 10^{19} \times 1.6 \times 10^{-19}(0.39 + 0.19) \times 10^{-6}}$$

$$= 4000\ \Omega = 4\ \text{k}\Omega$$

10. Conductivity of semiconductor is given by

$$\sigma = n_e e\mu_e + n_h e\mu_h$$

Since semiconductor is intrinsic

$\Rightarrow \quad n_e = n_h = n_i$

or $\sigma = n_i e(\mu_e + \mu_h)$

$$= 1.6 \times 10^6 \times 1.6 \times 10^{-19}\ (0.4 + 0.2)$$

$$= 1.536 \times 10^{-13}\ \Omega^{-1}\text{m}^{-1}$$

Current flowing, $I = jA$ ...(i)

where, j = current density $= \sigma E = \sigma\left(\dfrac{V}{d}\right)$

From Eq. (i), we get

$$I = 1.536 \times 10^{-13}\left(\frac{5}{1.5 \times 10^{-3}}\right)(3.5 \times 10^{-4})$$

$$= 1.79 \times 10^{-13}\ \text{A}$$

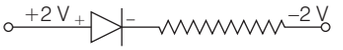
Heat produced, $H = VIt = 5 \times 1.79 \times 10^{-13} \times 120$

$$= 10.74 \times 10^{-11}\ \text{J}$$

11. In circuit 1, n is connected with n, which is not a series combination of p-n junction. In circuit 2, each p-n junction is forward biased, same current flows, giving same potential difference across junction. In circuit 3, each p-n junction is reverse biased, same leakage current will flow, giving equal potential difference across each p-n junction diode.

12. V-d curve near the junction will be as shown by curve (a).

13. For forward bias, p-side must be a higher potential than n-side.

So, 

is forward biased.

14. When p-n junction is forward biased, it opposes the potential barrier across junction. When p-n junction is reverse biased, it supports the potential barrier junction, resulting increases in potential barrier across the junction. Thus, option (b) is correct.

15. Potential drop in a silicon diode in forward bias is around 0.7 V.

In given circuit, potential drop across 200 Ω resistor is

$$I = \frac{\Delta V_{\text{net}}}{R} = \frac{3 - 0.7}{200}$$

$\Rightarrow \quad I = 0.0115\ \text{A} \quad \Rightarrow \quad I = 11.5\ \text{mA}$

16. In the given circuit, p side of p-n junction D_1 is connected to lower voltage and n-side of D_1 to higher voltage. Therefore, D_1 is reverse biased. The p-side of p-n junction D_2 is at higher potential and n-side of D_2 is at lower potential. Therefore, D_2 is forward biased.

Due to reverse biasing of diode D_1, circuit becomes open. Hence, no current flows through the junction from B to A, *i.e.* option (b) is correct.

17. As, $R_e = \dfrac{\Delta V}{\Delta I} = \dfrac{(13-8)}{(60-40)\times 10^{-6}} = 2.5\times 10^5\ \Omega$

18. In reverse biasing, the minority charge carriers will be accelerated due to reverse biasing, which on striking with atoms cause ionisation resulting secondary electrons and thus more number of charge carriers.

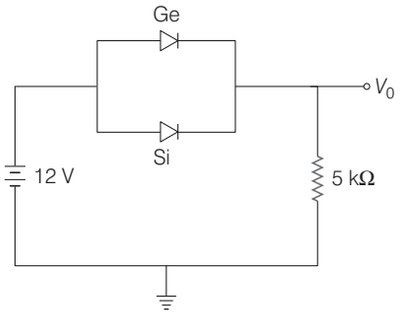
When doping concentration is large, there will be large number of ions in the depletion region, which will give rise to a strong electric field.

19. Let V be the potential difference between A and B, then

$$V - 0.3 = (5+5)\times 10^3 \times (0.2\times 10^{-3}) = 2$$

or $$V = 2 + 0.3 = 2.3\ \text{V}$$

20. Initially Ge and Si are both forward biased, so current will effectively pass through Ge diode with a voltage drop of 0.3 V.

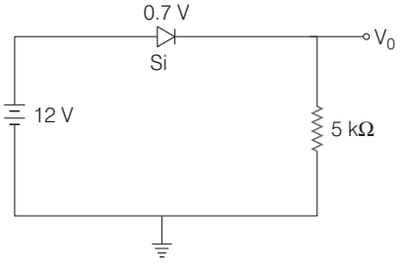


$\therefore$ Initial output voltage,

$$V_0 = 12 - 0.3 = 11.7\ \text{V}$$

If Ge is reversed biased, then only Si diode will work. In this condition, output voltage

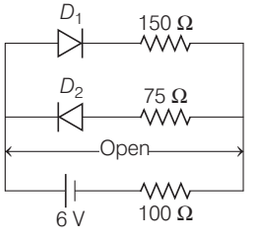
$$V_0 = 12 - 0.7 = 11.3\ \text{V}$$



$\therefore$ Change in output voltage

$$= 11.7 - 11.3 = 0.4\ \text{V}$$

21. In this circuit, D_1 is forward biased and D_2 is reversed biased.



Resistance of D_1 is 50 Ω.

$\therefore$ Net resistance of the circuit,

$$R_{\text{net}} = 50 + 150 + 100 = 300\ \Omega$$

$\therefore$ Current through the 100 Ω resistance

$$= \frac{V}{R_{\text{net}}} = \frac{6}{300} = 0.020\ \text{A}$$

22. During positive half cycle of input AC voltage, the p-n junction is forward biased. The resistance of p-n junction is low. The current in the circuit is maximum. In this situation, a maximum potential difference will appear across resistance connected in series of circuit. Due to it, there is no output voltage across p-n junction.

During the negative half-cycle of input AC voltage, the p-n junction is reverse biased. The resistance of p-n junction becomes high which will be more than resistance in series. Due to it, there will be voltage across p-n junction with negative cycle in output.

23. Here, $V = (50\sin\omega t)$ volt

Comparing it with general equation $V = V_0 \sin\omega t$, we get

$$V_0 = 50\ \text{V},\ R_L = 650\ \Omega,\ \ r_d = 200\ \Omega$$

Maximum output current, $I_0 = \dfrac{V_0}{r_d + R_L} = \dfrac{50}{(200+650)}$

$$= 58\ \text{mA}$$

DC output current, $I_{\text{DC}} = \dfrac{I_0}{\pi} = \dfrac{58\times 7}{22} = 18.5\ \text{mA}$

DC output power $= I_{\text{DC}}^2 \cdot R_L = (18.5)^2 \times 650 = 0.22\ \text{W}$

24. For same value of current, higher value of voltage is required for higher frequency.

Since, $\nu_B > \nu_G > \nu_Y > \nu_R$

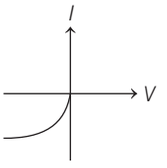
Hence, $V_B > V_G > V_Y > CV_R$

25. Photons are detected by photodiode, so band gap energy is given by

$$\Delta E = \frac{hc}{\lambda} \Rightarrow \Delta E = \frac{1240\ \text{eV-nm}}{400\ \text{nm}} = 3.1\ \text{eV}$$

Note $hc \approx 1240$ eV-nm

26. The I-V characteristic curve for a photodiode is shown below



With increasing biasing voltage of a photodiode, the photocurrent first increases and then becomes saturated, *i.e.* after certain potential, electron-hole pair production will be nearly constant.

Hence, correct option is (b).

27. Energy of incident light (photon),

$$h\nu = \frac{hc}{\lambda} = \frac{6.6\times 10^{-34}\times 3\times 10^8}{6\times 10^{-7}\times 1.6\times 10^{-19}} = 2.06\ \text{eV}$$

For the incident radiation to be detected by the photodiode, energy of incident radiation (photon) should be greater than the band gap. This is true only for D_2.

28. Zener diode works in breakdown region.

So, Simple diode → (a)

Zener diode → (b)

Solar cell → (c)

Light dependent resistance → (d)

29. When the applied reverse voltage V reaches the breakdown voltage of the Zener diode, then only a large amount of current is flown through it, otherwise it is approximately zero.

In the given situation, if we consider that Zener diode is at breakdown, then potential drop across 1500 Ω resistances will be 10 V. So, potential drop at 500 Ω resistor will be 2 V.

$\therefore$ Current in $R_1 = \dfrac{2}{500} = 4\text{mA} = I_1$ (say)

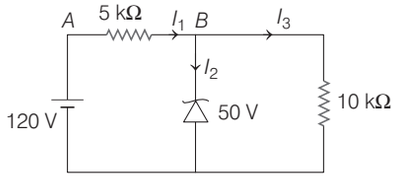
Current in each $R_2 = \dfrac{10}{750} = \dfrac{2}{150} = 13.33\text{ mA} = I_2$ (say)

$\Rightarrow$ $I_1 < I_2$ which is not possible.

So, Zener diode will never reach to its breakdown.

$\therefore$ Current flowing through a reverse biased Zener diode = 0.

30. In the circuit, let the current in branches is as shown in figure below



By Kirchhoff's node law,

$$I_1 = I_2 + I_3 \quad \text{... (i)}$$

Now, when diode conducts, voltage difference between points A and B will be

$$V_{AB} = 120 - 50 = 70\text{ V}$$

So, current, $I_1 = \dfrac{V_{AB}}{5\text{ k}\Omega} = \dfrac{70}{5 \times 10^3}$

$$I_1 = 14\text{ mA} \quad \text{...(ii)}$$

Since, diode and 10 kΩ resistor are in parallel combination, so voltage across 10 k Ω resistor will be 50 V only.

$\Rightarrow$ $I_3 = \dfrac{50}{10\text{ k}\Omega} = \dfrac{50}{10 \times 10^3}$

$\Rightarrow$ $I_3 = 5\text{ mA}$ ... (iii)

$\therefore$ From Eqs. (i), (ii) and (iii), we get

$$14\text{ mA} = I_2 + 5\text{ mA}$$

or current through diode,

$$I_2 = 14\text{ mA} - 5\text{mA} = 9\text{ mA}$$

31. For $V < 4$V, both diodes are reverse biased but not working in Zener region. So, output voltage (V_{out}) will be equal to input voltage.

For voltages higher than 4 V, diode A will not conduct current but diode B will work in Zener region and large current will flow through it. So, potential will increase but some voltage drop will occur in connecting wires. So, slope of V_{out} *versus* t graph will get reduced.

Once both the diodes start working in Zener region, the output voltage will become 6 V and after that, it will not change.

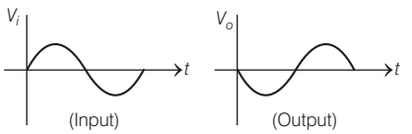
Hence, correct option is (c).

32. In an *n-p-n* transistor when base-emitter junction is forward biased and collector-base junction is reverse biased, the majority charge carriers electrons move from emitter-to-base. In base, few electrons get neutralised by electron-hole combination and the remaining electrons crossover the collector.

33. As, $\beta = \dfrac{I_C}{I_B} = \dfrac{I_E - I_B}{I_B} = \dfrac{I_E}{I_B} - 1$ or $\dfrac{I_E}{I_B} = 1 + \beta$

or $I_B = \dfrac{I_E}{1+\beta} = \dfrac{8.2}{1+40} = \dfrac{8.2}{41} = 0.20\text{ mA}$

34.



In a CE *n-p-n* transistor amplifier, output voltage is 180° out of phase with input voltage.

35. As we know,

In case of a common emitter configuration, DC current gain, $\alpha = \dfrac{I_C}{I_E}$.

where, I_C is collector current and I_E is emitter current.

AC current gain, $\beta = \dfrac{I_C}{I_B}$ ...(i)

where, I_B is base current.

Also, $I_E = I_B + I_C$ ...(ii)

Dividing Eq. (ii) by I_C, we get

$\Rightarrow$ $\dfrac{I_E}{I_C} = \dfrac{I_B}{I_C} + 1$ [from Eq. (i)]

$\Rightarrow$ $\dfrac{1}{\alpha} = \dfrac{1}{\beta} + 1 \Rightarrow \alpha = \dfrac{\beta}{1+\beta}$

36. As, collector current, $I_C = \dfrac{90}{100} \times I_E$

where, I_E = emitter current.

$\Rightarrow$ $10 = 0.9 \times I_E$

$\Rightarrow$ $I_E = 11\text{ mA}$

Also, $I_E = I_B + I_C$

Base current, $I_B = I_E - I_C$

$= 11 - 10 = 1\text{ mA}$

37. Given, $\beta = 50$, $R_i = 1000\Omega$, $V_i = 0.01$ V

$$\beta = \frac{I_C}{I_B} \quad \text{... (i)}$$

and $$I_B = \frac{V_i}{R_i} = \frac{0.01}{10^3} = 10^{-5} \text{ A}$$

$$I_C = 50 \times 10^{-5} \text{ A} = 500\,\mu\text{A} \quad \text{[from Eq. (i)]}$$

38. Number of electrons reaching the collector,

$$n_C = \frac{96}{100} \times 10^{10} = 0.96 \times 10^{10}$$

Emitter current, $I_E = \frac{n_E \times e}{t}$

Collector current, $I_C = \frac{n_C \times e}{t}$

Thus, current transfer ratio,

$$\alpha = \frac{I_C}{I_E} = \frac{n_C}{n_E} = \frac{0.96 \times 10^{10}}{10^{10}} = 0.96$$

39. Input signal of a CE amplifier, $V_i = 2\cos\left(15t + \frac{\pi}{3}\right)$

Voltage gain, $A_V = 150$

As CE amplifier gives phase difference of π between input and output signals.

So, $$A_V = \frac{V_o}{V_i}$$

$\Rightarrow$ $$V_o = A_V V_i$$

$$V_o = 150 \times 2\cos\left(15t + \frac{\pi}{3} + \pi\right)$$

Output signal, $V_o = 300\cos\left(15t + \frac{4\pi}{3}\right)$

40. Here, $I_C = 10$ mA

$\therefore$ $$I_C = \frac{95}{100} I_E \Rightarrow 10 \text{ mA} = \frac{95}{100} I_E$$

or $$I_E = \frac{100 \times 10}{95} = 10.53 \text{ mA}$$

$\Rightarrow$ $$i_C = \frac{2}{2 \times 10^3} = 10^{-3} \text{ A}$$

$\therefore$ Current gain, $\beta = \frac{i_C}{i_B}$

$$100 = \frac{10^{-3}}{i_B} \Rightarrow i_B = 10^{-5} \text{ A}$$

41. From the given transfer characteristics of a base biased common emitter transistor, we note that

(a) When $V_i = 0.4$ V, there is no collector current. The transistor circuit is in cut-off state.

(b) When $V_i = 1$ V (which is in between 0.6 V to 2 V), the transistor circuit is in active state and it used as an amplifier.

(c) When $V_i = 0.5$ V, there is no collector current. The transistor is in cut-off state. The transistor circuit can be used as a switch turned OFF.

(d) When $V_i = 2.5$ V, the collector current becomes maximum and transistor is in saturation state and can be used as switch turned ON state.

42. Given, $A_P = 60$ dB (in decibel)

Power gain in decibel can be given as

$$A_P = 10\log_{10}\left(\frac{\text{Output power}}{\text{Input power}}\right)$$

$\Rightarrow$ $$60 = 10\log_{10}\left(\frac{P_{\text{out}}}{P_{\text{in}}}\right) \Rightarrow \log_{10}\left(\frac{P_{\text{out}}}{P_{\text{in}}}\right) = 6$$

$\Rightarrow$ $$\frac{P_{\text{out}}}{P_{\text{in}}} = 10^6 = A_P \quad \text{... (i)}$$

Also, given $R_{\text{out}} = 10$ kΩ, $R_{\text{in}} = 100\,\Omega$

$\therefore$ Power gain of a transistor is given by

$$A_P = \beta^2\left(\frac{R_{\text{out}}}{R_{\text{in}}}\right)$$

where, β is current gain.

$\Rightarrow$ $$\beta^2 = A_P \times \frac{R_{\text{in}}}{R_{\text{out}}} = 10^6 \times \frac{100}{10 \times 10^3}$$

$\Rightarrow$ $$\beta^2 = 10^4 \text{ or } \beta = 10^2$$

43. Given curve is between I_C and I_B as output and input currents, respectively.

So, it is transfer characteristics curve of a common emitter (CE) configuration.

In CE configuration,

Current gain, $\beta = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{I_C}{I_B}$ ...(i)

Voltage gain,

$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{I_C \times R_{\text{out}}}{I_B \times R_{\text{in}}} = \beta \times \frac{R_{\text{out}}}{R_{\text{in}}} \quad \text{...(ii)}$$

and power gain,

$$A_P = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_C^2 \times R_{\text{out}}}{I_B^2 \times R_{\text{in}}} = \beta^2 \times \frac{R_{\text{out}}}{R_{\text{in}}} \quad \text{...(iii)}$$

Given, $R_{\text{in}} = 100\ \Omega$ and $R_{\text{out}} = 100 \times 10^3\ \Omega$

From Eq. (i), we get

$$\beta = \frac{5\,\text{mA}}{100\,\mu\text{A}}\left(\text{or } \frac{10\text{ mA}}{200\,\mu\text{A}} \text{ or } \frac{15\,\text{mA}}{300\,\mu\text{A}} \text{ or } \frac{20\,\text{mA}}{400\,\mu\text{A}}\right)$$

$\Rightarrow$ $$\beta = \frac{5 \times 10^{-3}}{100 \times 10^{-6}} = 50 \quad \text{...(iv)}$$

From Eqs. (ii) and (iv), we get

Voltage gain, $A_V = \beta \times \frac{R_{\text{out}}}{R_{\text{in}}} = 50 \times \frac{100 \times 10^3}{100}$

$\Rightarrow$ $$A_V = 50000 = 5 \times 10^4 \quad \text{...(v)}$$

From Eqs. (iii) and (iv), we get

Power gain, $A_P = \beta^2 \times \frac{R_{\text{out}}}{R_{\text{in}}} = (50)^2 \times \frac{100 \times 10^3}{100}$

$$= 2500 \times 1000$$

$\Rightarrow$ $$A_P = 2.5 \times 10^6$$

44. For a common emitter *n-p-n* transistor, DC current gain,

$$\beta_{\text{DC}} = \frac{I_C}{I_B}$$

At saturation state, V_{CE} becomes zero.

$\therefore \quad V_{CC} - I_C R_C = 0$

$$I_C \approx \frac{V_{CC}}{R_C} = \frac{10}{1000} = 10^{-2}\text{A}$$

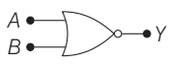
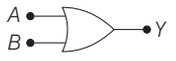
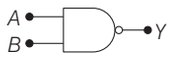
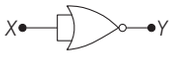
Hence, saturation base current,

$$I_B = \frac{I_C}{\beta_{DC}} = \frac{10^{-2}}{250} = 40\,\mu\text{A}$$

45. When S_1 is put ON to apply proper bias for the first time in the given circuit. Obviously, a surge of collector current flows in the transistor. This current flows through the coil T_2 where terminals are numbered 3 and 4 in the circuit. This current does not reach full amplitude instantaneously but increases from X to Y, as shown in Fig (i).

The inductive coupling between coil T_2 and coil T_1 now causes a current to flow in the emitter circuit (**Note** that this actually is the 'feedback' from input to output). As a result of this positive feedback, this current (in T_1; emitter current) also increases from X' to Y' as shown in Fig (ii). Thus, initially, both I_C and I_E increase.

46. Given gates and their truth tables are as below

1.		NOR gate	A B Y 0 0 1 1 0 0 0 1 0 1 1 0
2.		OR gate	A B Y 0 0 0 1 0 1 0 1 1 1 1 1
3.		NAND gate	A B Y 0 0 1 1 0 1 0 1 1 1 1 0
4.		One input NOR gate	X Y 0 1 1 0

Clearly, 4th gate converts a low voltage (0) into a high voltage (1) and *vice-versa.*

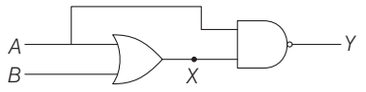
So, 4th gate or one input NOR gate gives a reversible operation.

47. From the figure, the truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

i. e. AND gate

48. Given circuit is



Let the intermediate state X of OR gate is shown in figure.

Clearly, $\quad Y = \overline{AX} \quad \ldots(i)$

Here, $\quad X = A + B \quad \ldots(ii)$

$\therefore \quad Y = \overline{A\,(A+B)} = \overline{AA + AB}$

$= \overline{A + AB} \qquad (\because AA = A)$

$= \overline{A\,(1+B)}$

$\Rightarrow \quad Y = \overline{A} \qquad (\because 1 + B = 1)$

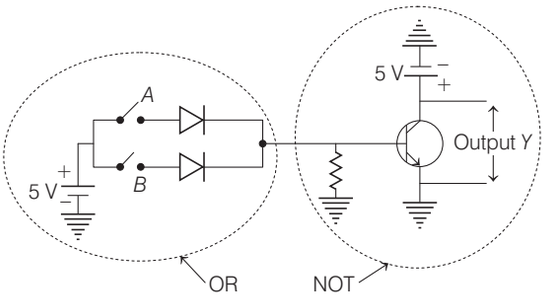
So, truth table shown in option (c) is correct.

49. Output of OR gate is 0 when all inputs are 0 and output is 1 when atleast one of the input is 1.

Observing output *x* It is 0 when all inputs are 0 and it is 1 when atleast one of the input is 1.

$\therefore$ The gate is OR.

50. Given circuit is a combination of OR gate and NOT gate.



So, given combination is a NOR gate, its truth table is

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

Its Boolean relation,

$$Y = \overline{A + B} = \overline{A} \cdot \overline{B} \qquad \text{(by de Morgan's rule)}$$

51. In circuit, $C = A \cdot B$ and $D = \overline{A} \cdot B$

$$E = C + D = (A \cdot B) + (\overline{A} + B)$$

Truth table of this arrangement of gates can be as given below

A	B	$\overline{A}$	$C = A \cdot B$	$D = \overline{A} \cdot B$	$E = (C + D)$
0	0	1	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	1	0	1	0	1

52. Output of gate I is $Y' = \overline{A + B}$

Output of gate II is $Y_1 = \overline{A + Y'}$

Output of gate III is $Y_2 = \overline{B + Y'}$

Output of gate IV is $Y = \overline{Y_1 + Y_2}$

$\Rightarrow \quad Y = \overline{\overline{A + Y}} + \overline{\overline{B + Y'}} = (A + Y')\,(B + Y')$

$= (A + Y')\,(B + Y')$

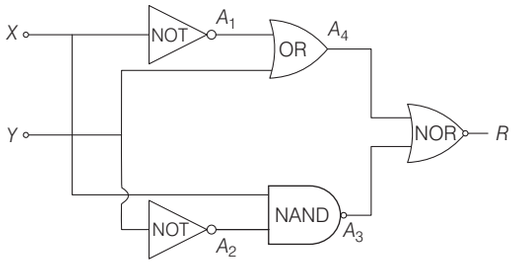
$\Rightarrow \quad Y = [A + \overline{A + B}]\,[B + \overline{A + B}] = (A + \overline{A} \cdot \overline{B})\,(B + \overline{A} \cdot \overline{B})$

$\Rightarrow \quad Y = AB + (A\overline{A})\overline{B} + \overline{A}\,\overline{B}B + (\overline{A}\,\overline{B}) \cdot (\overline{A}\,\overline{B})$

$\Rightarrow \quad Y = AB + 0 + 0 + \overline{A}\,\overline{B} + AB + \overline{A}\,\overline{B}$ = output of XNOR gate.

The truth table of the combination is in option (a).

53. The given circuit can be drawn as shown in the figure given below

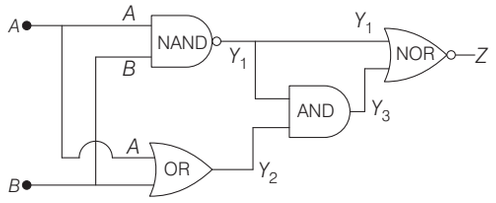


Truth table for this given logic gate is

Given inputs in the options		A_1	A_2	A_3	A_4	R
X	Y					
0	0	1	1	1	1	0
1	0	0	1	0	0	1
1	1	0	0	1	1	0
0	1	1	0	1	1	0

So to get output $R = 1$, inputs must be $X = 1$ and $Y = 0$.

54. The digital circuit having different components is shown below,

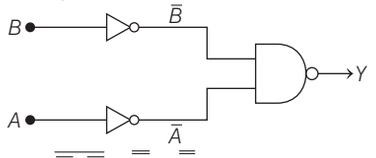


Truth table of above circuit is

A	B	$Y_1 = \overline{A \cdot B}$	$Y_2 = A + B$	$Y_3 = Y_1 \cdot Y_2$	$Z = \overline{Y_1 + Y_3}$
1	0	1	1	1	0
0	0	1	0	0	0
1	1	0	1	0	1
0	1	1	1	1	0

Hence, correct option is (a).

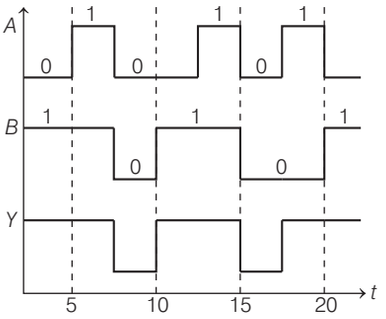
55. Given circuit,



Output, $Y = \overline{\bar{A} \cdot \bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$

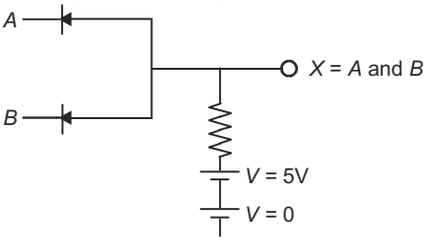
Truth Table

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

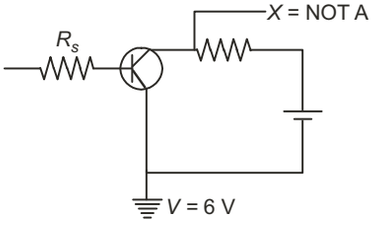


So, most appropriate option is (b).

56. From the figure of AND gate



and NOT gate



Clearly, the function X = NOT (A AND B) of the logical variables A AND B is called NAND gate.

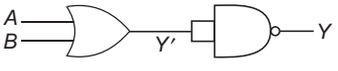
57. Truth table for the given logic gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

The truth table is similar to that of a NOR gate.

Round II

1. The output, $Y' = A + B$



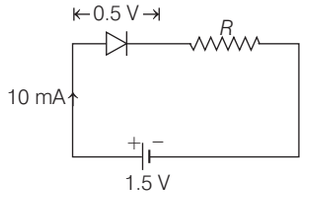
and $Y = \bar{Y}' = \overline{A + B}$

i.e. Output of a NOR gate.

2. The conditions for a circuit to oscillate are (i) the feedback is positive (ii) the fraction of the output voltage feedback, *i.e.* $\beta = \dfrac{1}{A}$, *i.e.* the reciprocal of the voltage gain without feedback.

3. During positive half cycle, p-n junction conducts. Potential difference across C = peak voltage of the given AC voltage = $V_0 = V_{\text{rms}} = \sqrt{2} = 220\sqrt{2}$ V.

4. Given circuit is

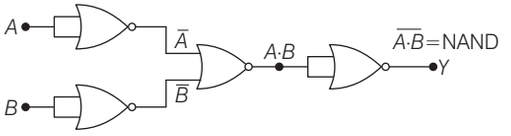


Now, by Kirchhoff 's loop rule,

$$1.5 - 0.5 - R \times 10 \times 10^{-3} = 0 \Rightarrow R = 100\,\Omega$$

5. When diode is reverse biased, the applied voltage supports the barrier voltage. Due to it, the reverse current is weak. It will be identical in two diodes.

6. By De-Morgan's theorem, we have



7. For $V_i < 0$,

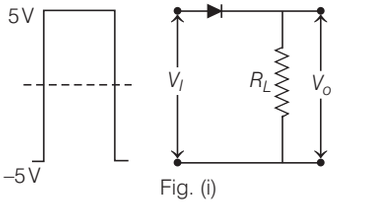


Fig. (i)

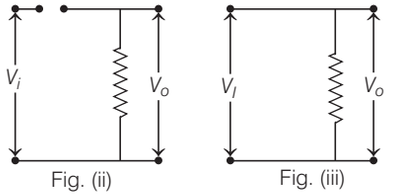


Fig. (ii)

Fig. (iii)

The diode is reverse biased and hence offer infinite resistance, so, circuit would be like as shown in Fig. (ii) and $V_o = 0$. For $V_i > 0$, the diode is forward biased and circuit would be as shown in Fig. (iii) and $V_o = V_i$.

8. Here p-n junction is forward biased. If p-n junction is ideal, its resistance is zero. The effective resistance across A and B

$$= \frac{10 \times 10}{10 + 10} = 5\ \text{k}\Omega$$

Current in the circuit, $I = \frac{V}{R} = \frac{30}{15 \times 10^3} = \frac{2}{10^3}\ \text{A}$

Current in arm AB, $I = \frac{2}{10^3}$

Potential difference across A and B

$$= \frac{2}{10^3} \times 5 \times 10^3 = 10\ \text{V}$$

9. Voltage gain, $A_V = \beta \frac{R_2}{R_1}$

Also, current gain, $\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$

$$A_V = 49\left(\frac{500 \times 10^3}{R_1}\right) \quad \ldots(\text{i})$$

$\therefore$ Power gain $= 6.0625 \times 10^6$ …(ii)

From Eqs. (i) and (ii), we get

$$\frac{49 \times 500 \times 10^3}{R_1} = 6.0625 \times 10^6$$

$$\Rightarrow \quad R_1 = \frac{49 \times 5 \times 10^5}{6.0625 \times 10^6}$$

$$\therefore \quad R_1 = 404.37400$$

10. Output of $G_1 = (A + B)$

Output of $G_2 = \overline{A \cdot B}$

Output of $G_3 = (A + B) \cdot \overline{A \cdot B} = (A + B)(\overline{A} + \overline{B})$

$$= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B}$$
$$= O + A\overline{B} + B\overline{A} + 0 = A\overline{B} + \overline{A}B$$

which give XOR gate.

11. Current through circuit,

$$I = \frac{P}{V} = \frac{100 \times 10^{-3}}{0.5} = 0.2\ \text{A}$$

Voltage drop across $R = 1.5 - 0.5 = 1.0$ V

Hence, $R = 1/0.2 = 5\,\Omega$

12. The given circuit works as half-wave rectifier. In this circuit, we will get current through R when p-n junction diode is forward biased and there is no current when p-n junction is reversed biased. Thus, the current through resistance will be shown by graph (b).

13. At logic gate I, the Boolean expression is

$$\overline{B} \cdot C = Y'$$

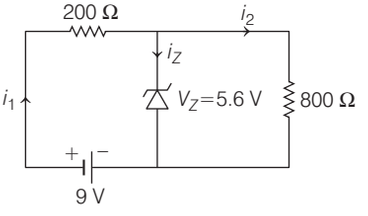
At logic gate II, the Boolean expression is

$$A + (\overline{B} \cdot C) = Y''$$

At logic gate III, the Boolean expression is

$$\overline{A + (\overline{B} \cdot C)} = Y$$

14. Given circuit is Zener diode circuit.



where,potential drop across 800 Ω resistance = potential drop across Zener diode = 5.6 V.

So, current, $i_2 = \frac{V}{R} = \frac{5.6}{800} = 7\text{mA}$

Now, potential drop across 200 Ω resistance

$$= 9 - 5.6 = 3.4\ \text{V}$$

Current, $i_1 = \frac{V}{R} = \frac{3.4}{200} = 17\ \text{mA}$

So, current, $i_Z = i_1 - i_2 = 17 - 7 = 10\ \text{mA}$

$$\text{Current in } 100\,\Omega = \frac{6}{300} = 0.02\ \text{A}$$

15. Here Boolean expression is $Y = \overline{(A + B)\cdot C}$. So,

$Y = \overline{A\cdot B} = \overline{0.1} = 1$ as the Boolean expression of it is $Y = \overline{A\cdot B}$ (for NAND gate).

Hence, when $A = B = 1$, $C = \overline{AB} = \overline{1\cdot 1} = \bar{1} = 0$

16. Zener diode is used to regulate voltage with any amount of increase in current while the change in voltage is negligible. This is well defined in the region *de*.

17. $A_V = \dfrac{\Delta V_o}{\Delta V_i} = \beta\dfrac{R_o}{R_i}$

So, $\Delta V_o = \Delta V_i \times \beta\dfrac{R_o}{R_i}$

$\therefore \quad \Delta V_o = 10 \times 50 \times \dfrac{5000}{2000} = 1250 \text{ mV} = 1.25 \text{ V}$

18. As, $V_B = V_{\text{knee}} + IR$

or $4 = 0.7 + 10^{-3} R$

or $R = 3.3/10^{-3} = 3.3 \times 10^3\ \Omega = 3.3\ \text{k}\Omega$

19. $f_{\text{out}} = 2\, f_{\text{input}} = 2 \times 50 = 100\ \text{Hz}$

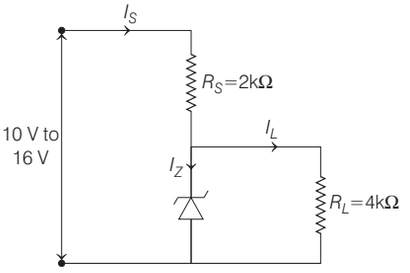
Mobility of electrons is 2 to 3 times larger than that of hole. Hence, $\mu_e > \mu_h$.

Current gain $\beta = 100$ and $\alpha = \dfrac{\beta}{1+\beta} = \dfrac{100}{101}$;

Given, $\dfrac{\Delta i_C}{\Delta i_E} = \dfrac{100}{101} = \dfrac{1\,\text{mA}}{\Delta i_E}$

$\therefore \quad \Delta i_E = 1.01\ \text{mA}$

20. In given voltage regulator circuit, breakdown of Zener occurs at 6 V.



After breakdown, voltage across load resistance ($R_L = 4\text{k}\Omega$),

$V = V_Z = 6\text{V}$

$\therefore$ Load current after breakdown,

$$I_L = \frac{V_Z}{R_L} = \frac{6}{4000} = 1.5 \times 10^{-3}\ \text{A}$$

When unregulated supply is of 16 V, potential drop occurring across series resistance ($R_S = 2\ \text{k}\Omega$),

$V_S = V - V_Z$

$= 16 - 6 = 10\ \text{V}$

So, current across series resistance,

$$I_S = \frac{V_S}{R_S} = \frac{10}{2 \times 10^3} = 5 \times 10^{-3}\ \text{A}$$

So, current across Zener diode is

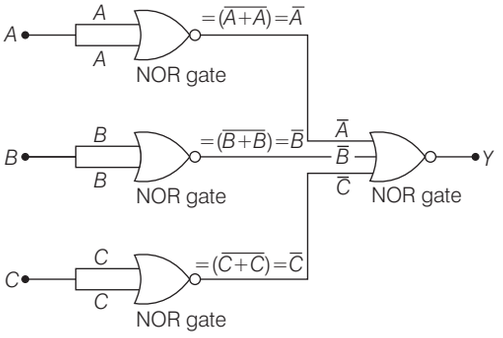
$I_Z = I_S - I_L$

$= 5 \times 10^{-3} - 1.5 \times 10^{-3}$

$= 3.5 \times 10^{-3}\ \text{A}$

$= 3.5\ \text{mA}$

21. Applying Boolean algebra,



$$Y = \overline{\overline{A} + \overline{B} + \overline{C}} = \overline{\overline{A}}\cdot\overline{\overline{B}}\cdot\overline{\overline{C}}$$

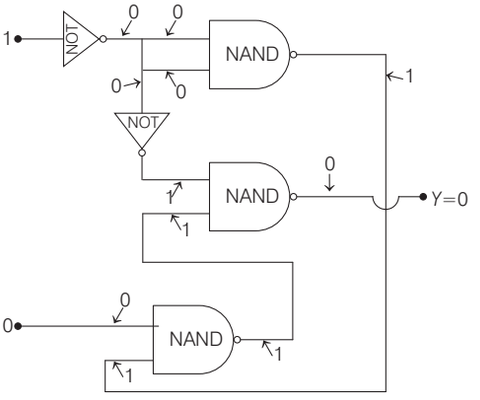
(Using de-Morgan's theorem)

$= A \cdot B \cdot C$

So, system behaves like AND gate.

Hence, option (a) is correct.

22. We are showing intermediate outputs on the circuit as given below



Output of above circuit at given inputs is zero.

To calculate output, we uses truth tables of NAND and NOT gates.

NAND gate

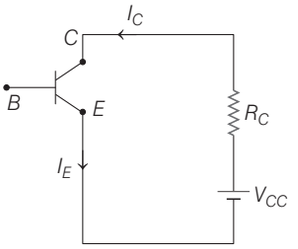
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

NOT gate

Y_{in}	Y_{out}
0	1
1	0

23. Transistor saturation occurs when $V_{CE} = 0$.

Now, for closed loop of collector and emitter by Kirchhoff's voltage rule, we have



$$V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow \quad 0 = V_{CC} - I_C R_c$$

$$\Rightarrow \quad I_C = \frac{V_{CC}}{R_C} = \frac{5}{1 \times 10^3} = 5 \times 10^{-3} \text{ A}$$

Now, $\beta_{DC} = 200$ (given)

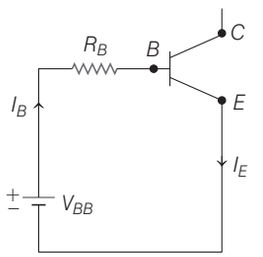
$$\Rightarrow \quad \frac{I_C}{I_B} = \beta_{DC} = 200$$

$$\Rightarrow \quad I_B = \frac{I_C}{200} = \frac{5 \times 10^{-3}}{200}$$

$$\Rightarrow \quad I_B = 2.5 \times 10^{-5} = 25\ \mu\text{A}$$

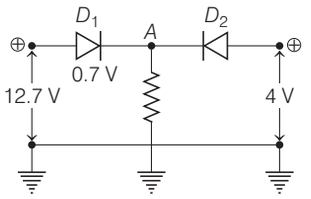
Now, we apply Kirchhoff's voltage rule in base-emitter closed loop, we get

$$V_{BB} = I_B R_B + V_{BE}$$



$$\Rightarrow \quad V_{BB} = (25 \times 10^{-6} \times 100 \times 10^3) + 1$$
$$= 3.5 \text{ V}$$

24. We have given circuit,



Diode D_1 is in forward bias and D_2 is in reverse bias, so D_1 conducts and D_2 resists.

$\therefore$ Potential at $A = 12.7 - 0.7 = 12$ V

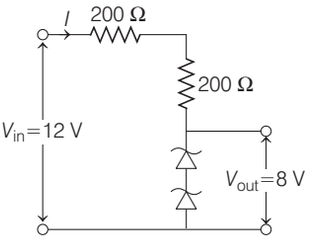
25. For a transistor, $\beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$

From given figure,

$$\Delta I_B = 30 - 20 = 10\ \mu\text{A}$$
$$\Delta I_C = 4.5 - 3 = 1.5\ \text{mA}$$

$$\therefore \quad \beta = \frac{1.5 \times 10^{-3}}{10 \times 10^{-6}} = 150$$

26. As input = 12 V and output = 8 V, this means 4V potential drop occurs in external resistance of 400 Ω.



So, current I across resistors, $= \frac{V}{R} = \frac{4}{400} = 10^{-2}$ A

As, there are two identical diodes and potential drop across diodes 8V, *i.e.* potential drop across each diode is 4V.

Hence, power dissipation across each diode,

$$P = VI = 4 \times 10^{-2} \text{ W} = 40 \text{ mW}$$

27. Given, collector resistance, $R_{output} = 2\ \text{k}\Omega = 2000\ \Omega$

Current amplification factor of the transistor, $\beta_{AC} = 100$

Audio signal voltage, $V_{output} = 2$ V

Input (base) resistance, $R_{input} = 1\ \text{k}\Omega = 1000\ \Omega$

$\because$ Voltage gain, $A_V = \frac{V_{output}}{V_{input}} = \beta_{AC} \frac{R_{output}}{R_{input}}$

$\therefore$ Input signal voltage, $V_{input} = \frac{V_{output}}{\beta_{AC}(R_{output}/R_{input})}$

$$= \frac{2}{100\,(2000/1000)}$$
$$= 0.01 \text{ V}$$

Base (input) current, $I_B = \frac{V_{input}}{R_{input}}$

$$= \frac{0.01}{1000}$$
$$= 10 \times 10^{-6} \text{ A}$$
$$= 10\ \mu\text{A}$$

28. Here, emf of the battery, $V = 2$ V, $l = 0.1$ m,

$$A = 1 \times 10^{-4} \text{m}^2$$

In case of silicon, $n_e = n_h = n = 1.5 \times 10^{16}/\text{m}^3$

Electric field, $E = \frac{V}{l}$, where emf of the battery $V = 2$ V and length of the block, $l = 0.1$ m

$$\Rightarrow \quad E = \frac{2\text{V}}{0.1\,\text{m}} = 20 \text{ V/m}$$

Clearly, $v_e = E\mu_e = 20 \times 0.135 \text{ m/s} = 2.70 \text{ m/s}$

$$v_h = E\mu_h = 20 \times 0.048 \text{ m/s} = 0.96 \text{ m/s}$$

Electron current,

$$I_e = eAn_e v_e = (1.6 \times 10^{-19})\ (10^{-4})\ (1.5 \times 10^{16})\ (2.70)$$
$$= 6.48 \times 10^{-7}\text{A}$$

Hole current,

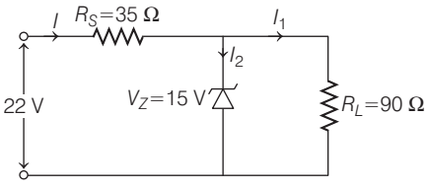
$$I_h = eAn_h v_h = (1.6 \times 10^{-19})\ (10^{-4})\ (1.5 \times 10^{16})\ (0.96)$$
$$= 2.304 \times 10^{-7}\text{A}$$

Total current,

$$I = I_e + I_h = (6.48 \times 10^{-7}\text{A}) + (2.304 \times 10^{-7}\text{A})$$
$$= 8.784 \times 10^{-7}\text{A}$$
$$= p \times 10^{-7}$$

$\therefore \quad p = 8.784$

29.



Voltage across $R_S = 22 - 15 = 7$ V

Current through R_S, $I = \frac{7}{35} = \frac{1}{5}$ A

Current through 90 Ω, $I_2 = \frac{15}{90} = \frac{1}{6}$ A

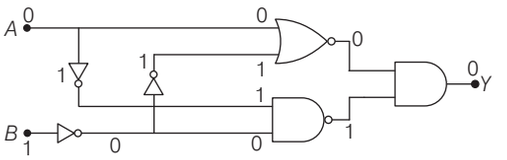
Current through zener, $\frac{1}{5} - \frac{1}{6} = \frac{1}{30}$ A

Power through zener diode,

$$P = VI$$
$$P = 15 \times \frac{1}{30} = 0.5\text{ W}$$
$$P = 5 \times 10^{-1}\text{ W}$$

The value of x is 5.

30.



The value of x is 0.